US006603874B1

(12) **United States Patent**
Stern et al.

(10) **Patent No.: US 6,603,874 B1**
(45) **Date of Patent: Aug. 5, 2003**

(54) **METHOD AND SYSTEM FOR IMAGING AN OBJECT OR PATTERN**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/518,559**

(22) Filed: **Mar. 3, 2000**

Related U.S. Application Data

(62) Division of application No. 08/748,040, filed on Nov. 12, 1996.

(51) **Int. Cl.**[7] **G06K 9/00**
(52) **U.S. Cl.** **382/144**; 382/149
(58) **Field of Search** 382/141, 144–151; 348/86, 87, 125, 126; 356/376, 237

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Assistant Examiner—Vikkram Bali
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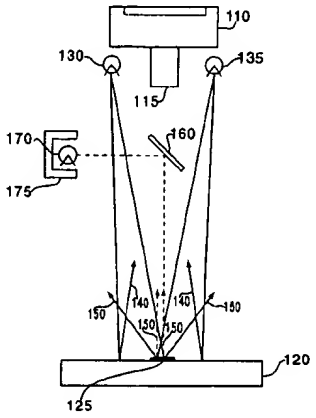
(57) **ABSTRACT**

A system and method for simultaneously obtaining a plurality of images of an object or pattern from a plurality of different viewpoints is provided. In an exemplary embodiment, proper image contrast is obtained by replacing the light sources of earlier systems with equivalent light sensitive devices and replacing the cameras of earlier systems with equivalent light sources. With such a system, bright-field images and dark-field images may be simultaneously obtained. In one aspect of the invention, a light source is positioned to illuminate at least a portion of an object. A plurality of light guides having input ends are positioned to simultaneously receive light reflected from the object and transmit the received light to a plurality of photodetectors. The light guides are arranged such that their respective input ends are spaced substantially equally along at least a portion of a surface of an imaginary hemisphere surrounding the object. The signals generated by the photodetectors (as a result of light detection) are processed and a plurality of images of the object are formed. Another aspect of the invention provides a method for generating composite images from simultaneously obtained images. Equivalent regions of each image (corresponding to geographically identical subpictures) are compared. The subpicture having the highest entropy is selected and stored. This process continues until all subpictures have been considered. A new composite picture is generated by pasting together the selected subpictures. In another aspect of the invention, the vector of relative light values gathered for each pixel or region of an object illuminated or scanned (i.e., one value for each photodetector) is used to determine reflectance properties of points or regions illuminated on the object or pattern. The reflectance properties may be stored in a matrix and the matrix used to read, for example, a Bar Code of a data matrix symbol.

6 Claims, 16 Drawing Sheets



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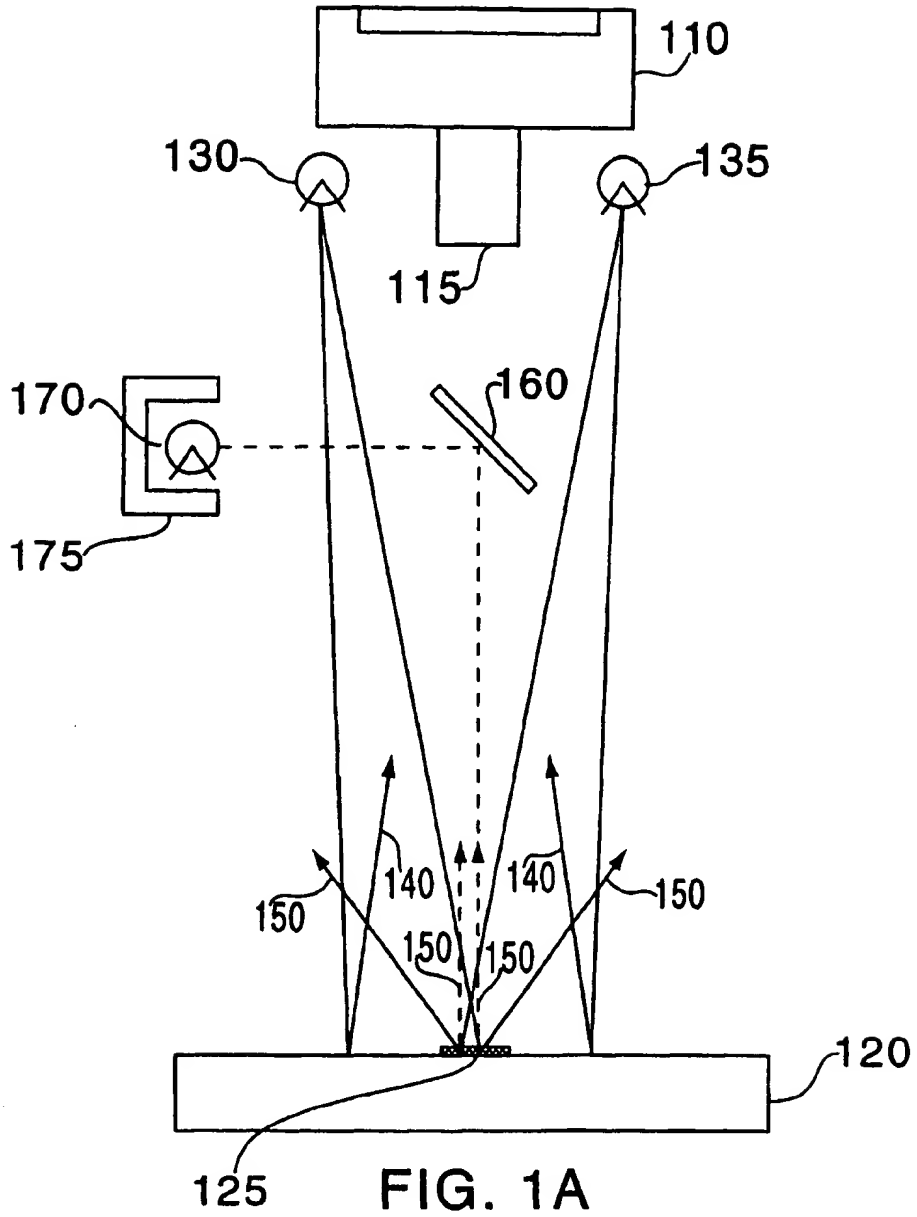

110
130
135
115
170
160
175
140
140
150
150
150
150
120
125

FIG. 1A

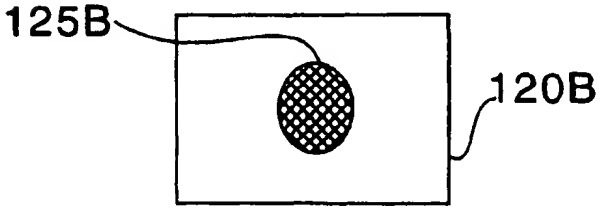
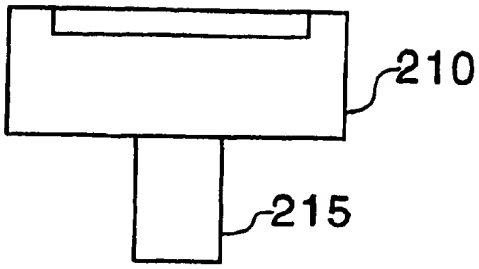

125B
120B

FIG. 1B



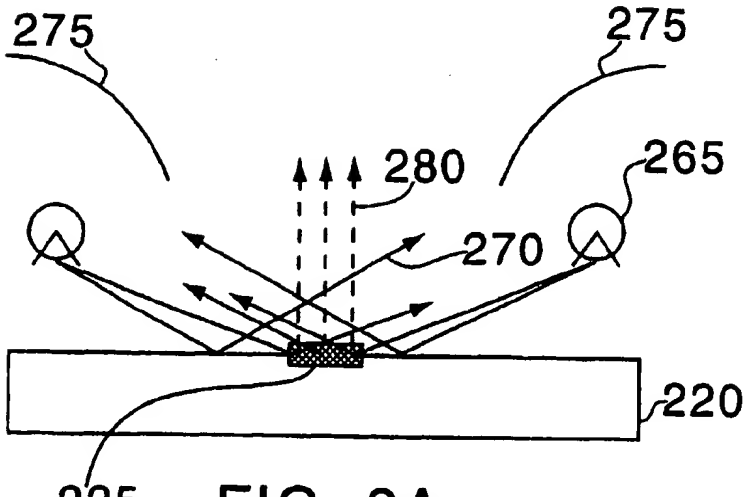


FIG. 2A

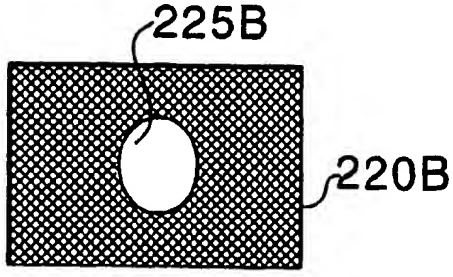


FIG. 2B

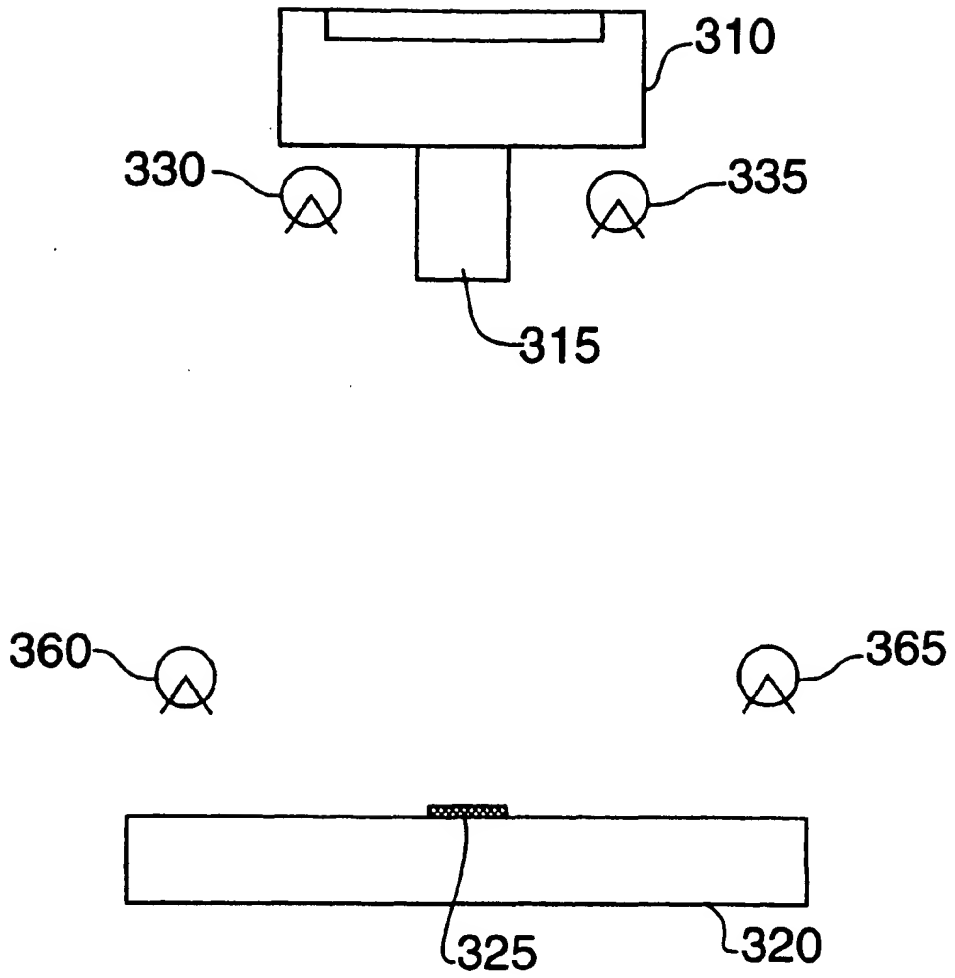


FIG. 3

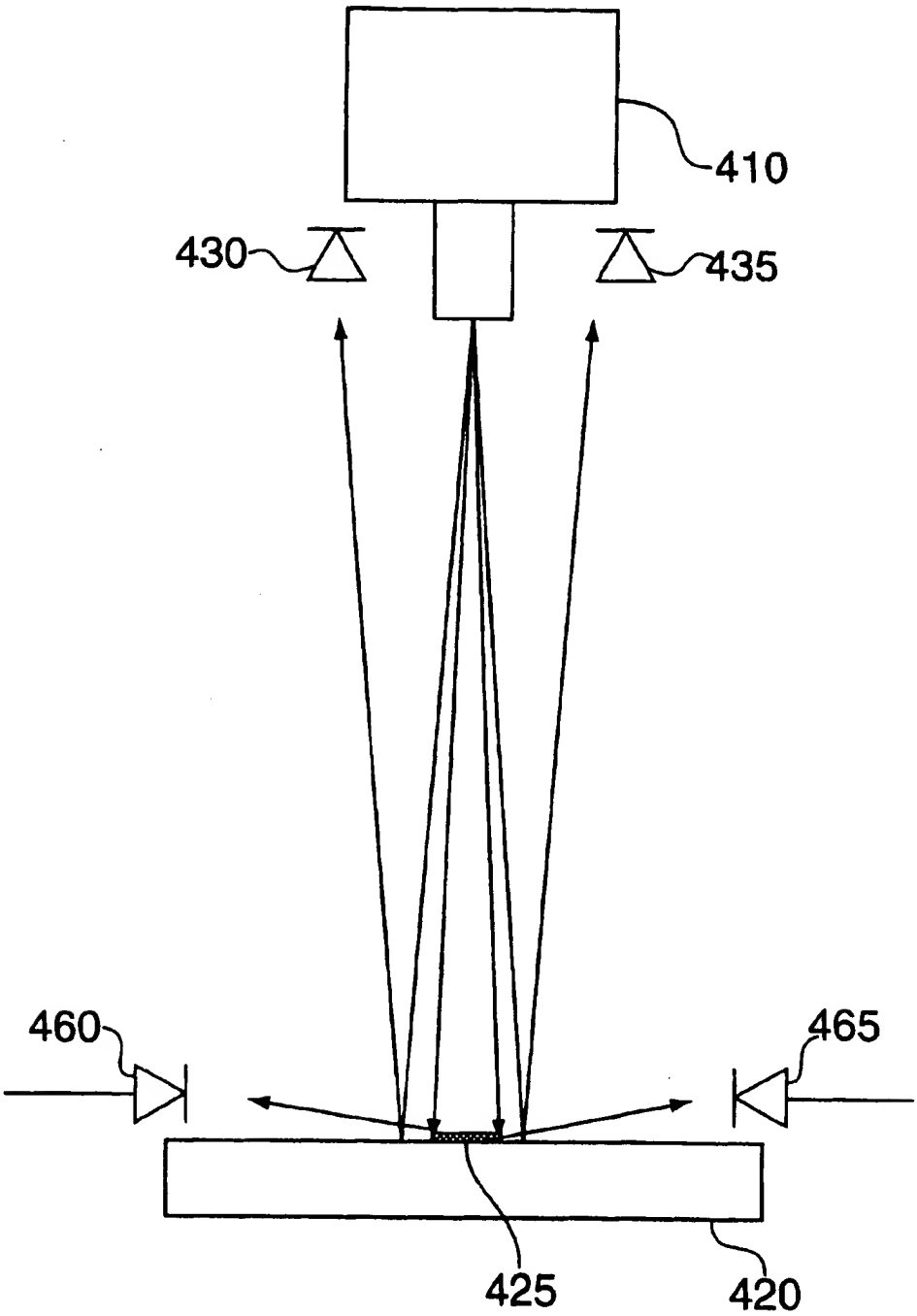


FIG. 4A

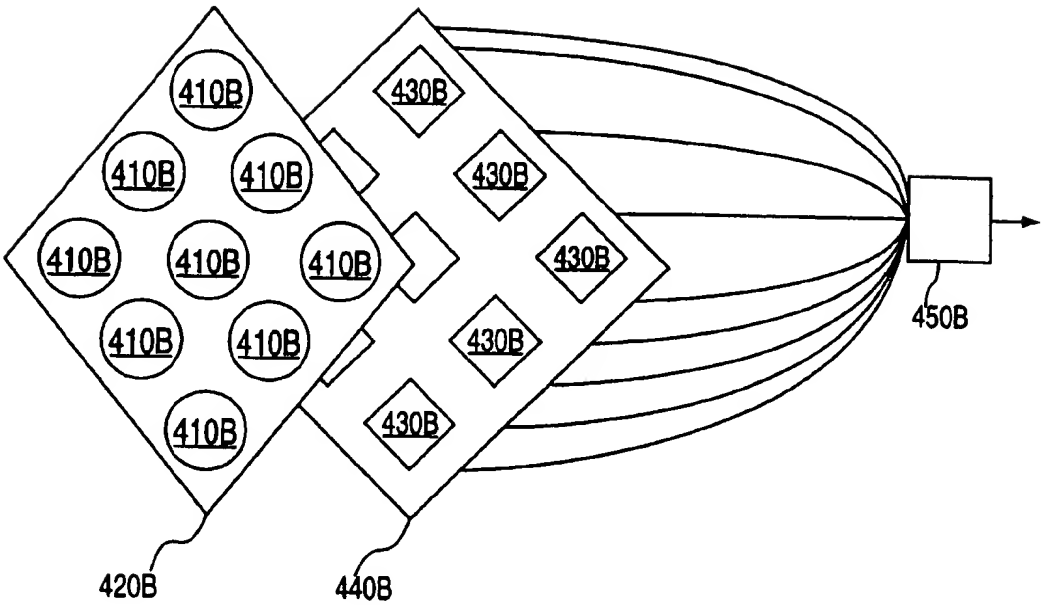

410B
410B
410B
410B
410B
410B
410B
410B
410B
430B
430B
430B
430B
430B
450B
420B
440B

FIG. 4B

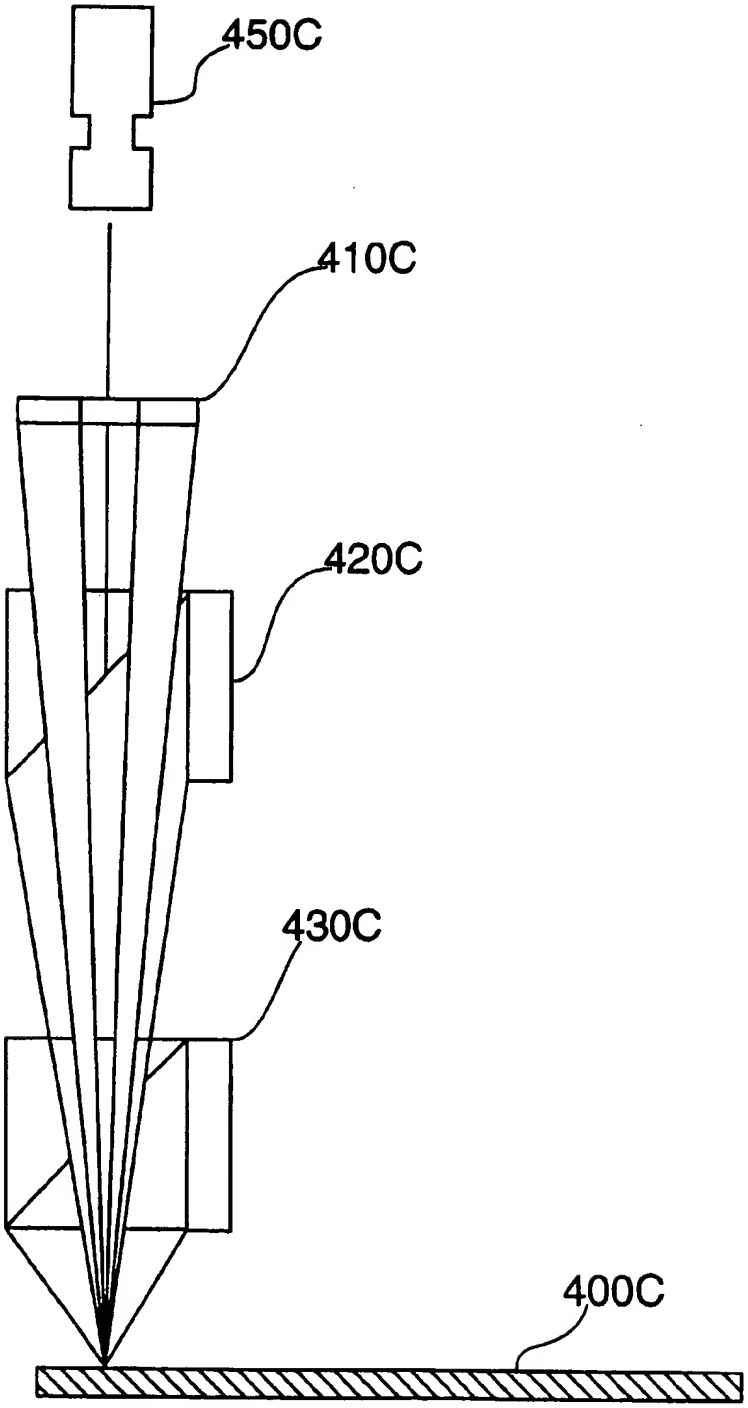


FIG. 4C

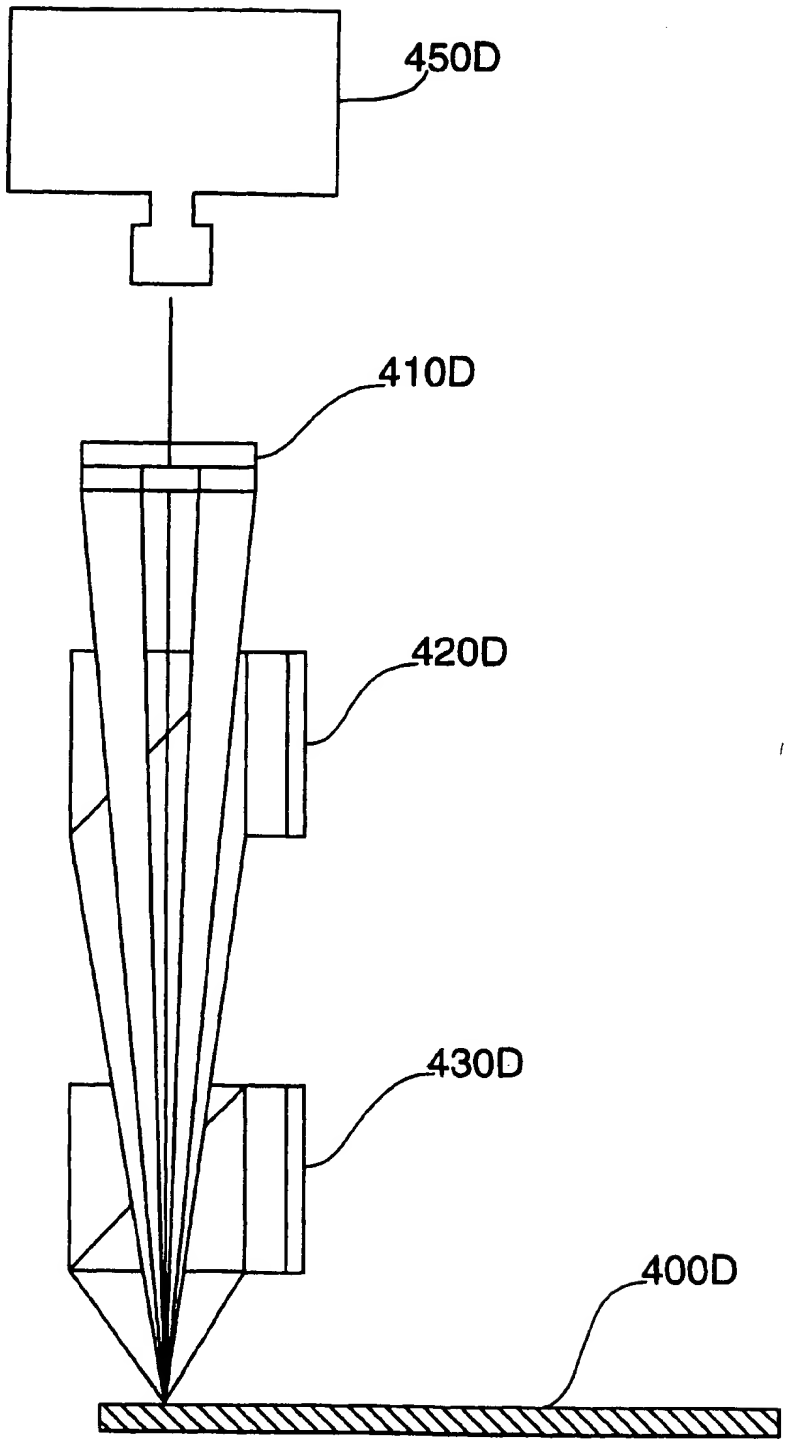


FIG. 4D

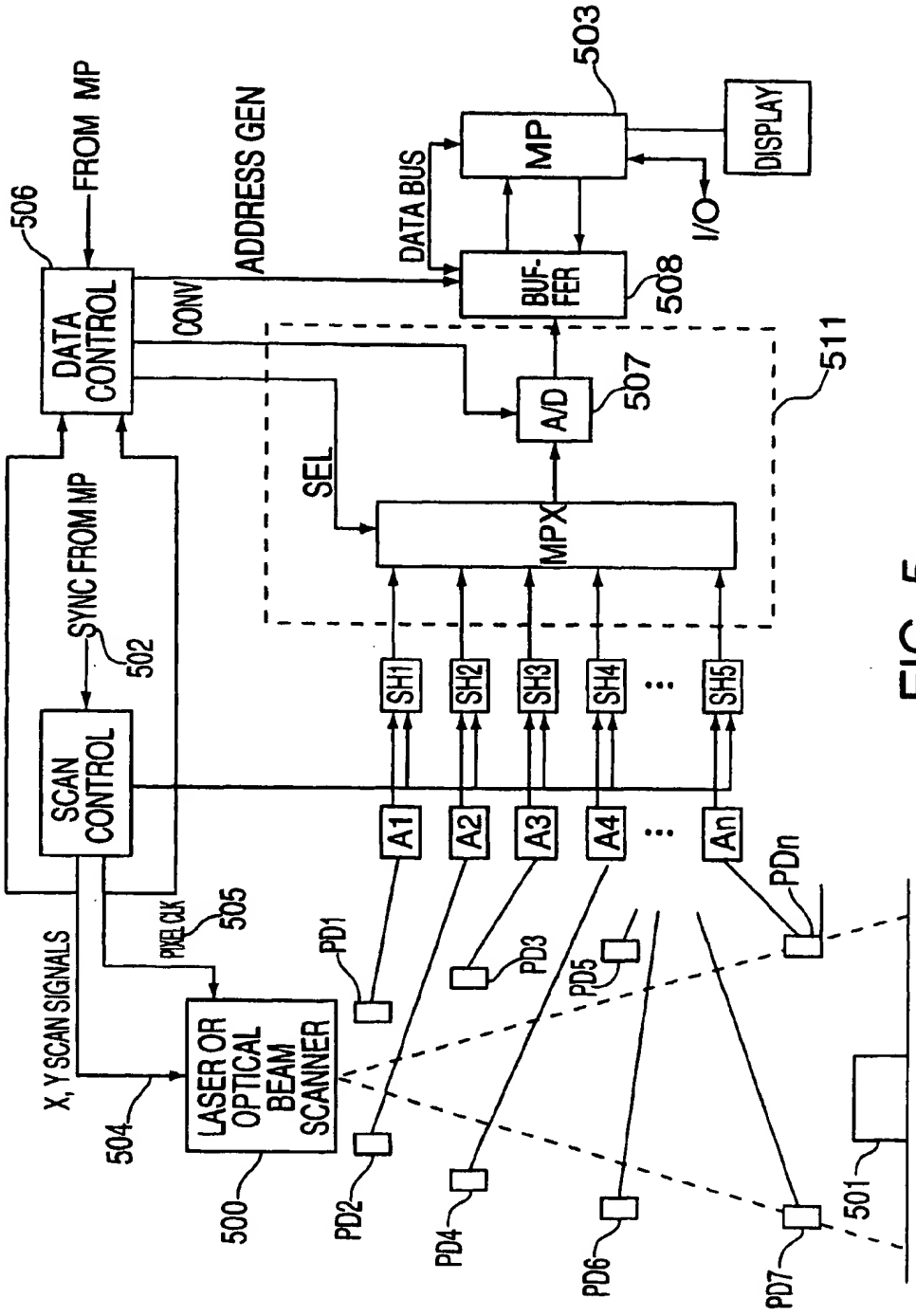

503
MP
DISPLAY
I/O
DATA BUS
FROM MP
506
ADDRESS GEN
DATA CONTROL
CONV
BUF-FER
508
511
A/D
507
SEL
MPX
SYNC FROM MP
502
SH1
SH2
SH3
SH4
SH5
SCAN CONTROL
A1
A2
A3
A4
An
PDn
PIXEL CLK
505
PD1
PD3
PD5
X, Y SCAN SIGNALS
LASER OR OPTICAL BEAM SCANNER
504
500
PD2
PD4
PD6
PD7
501

FIG. 5

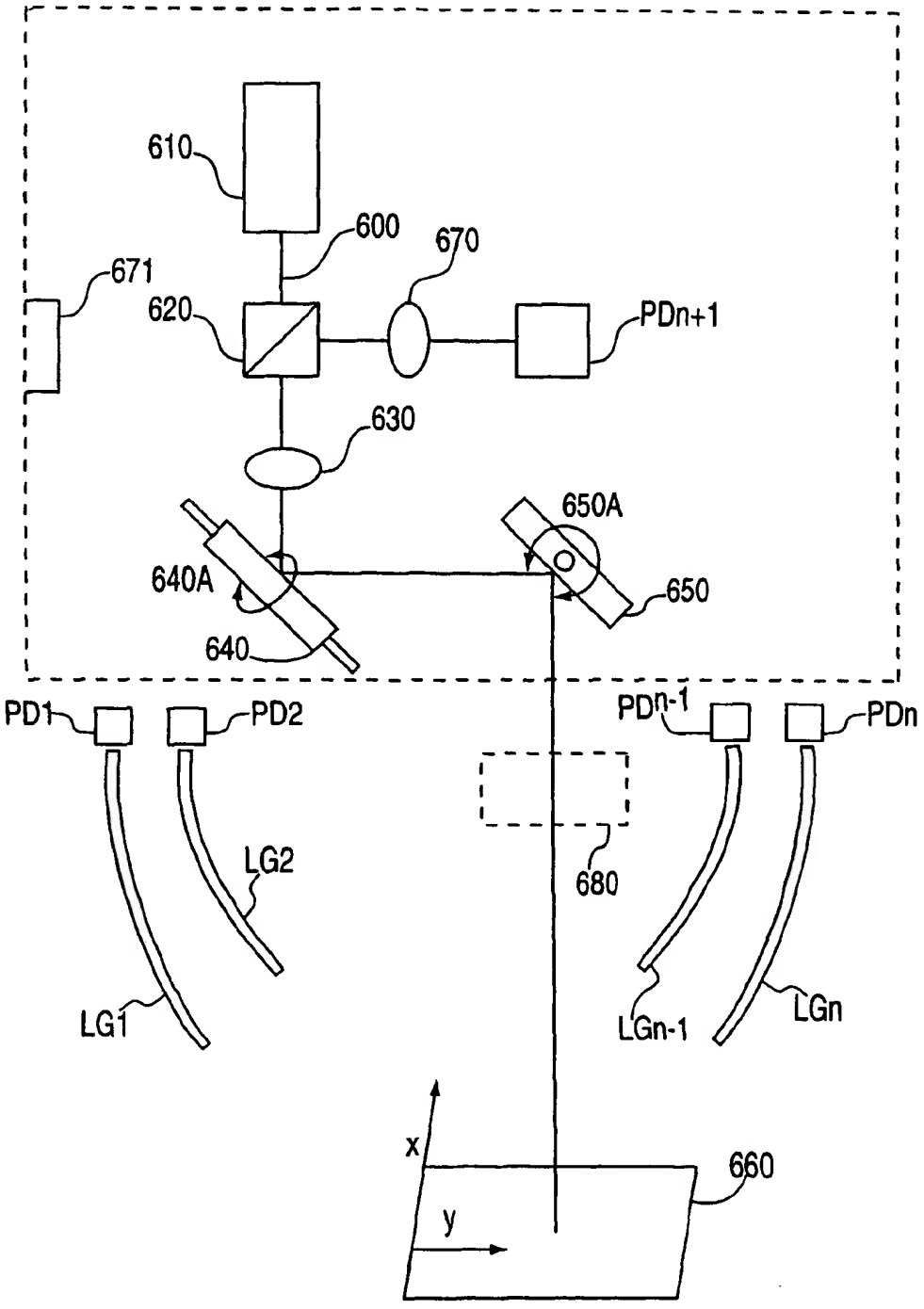

610
600
670
671
620
PDn+1
630
650A
640A
650
640
PD1
PD2
PDn-1
PDn
LG2
680
LG1
LGn-1
LGn
x
660
y

FIG. 6

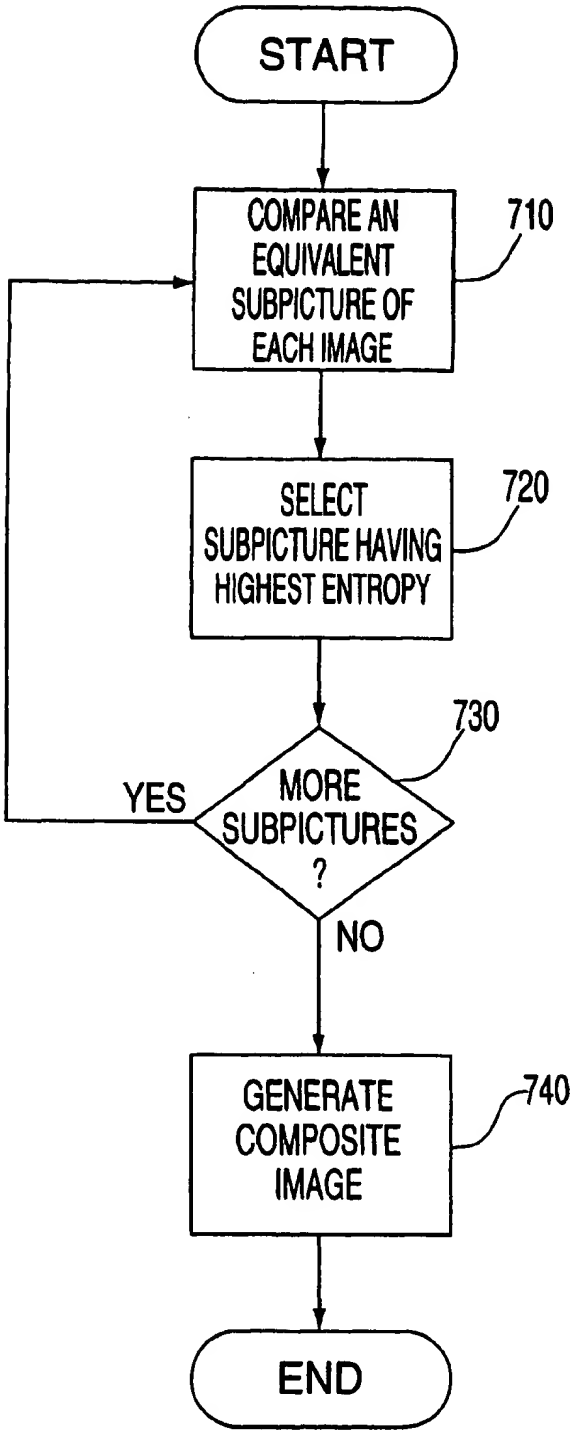

START
COMPARE AN EQUIVALENT SUBPICTURE OF EACH IMAGE
710
SELECT SUBPICTURE HAVING HIGHEST ENTROPY
720
730
MORE SUBPICTURES ?
YES
NO
GENERATE COMPOSITE IMAGE
740
END

FIG. 7A

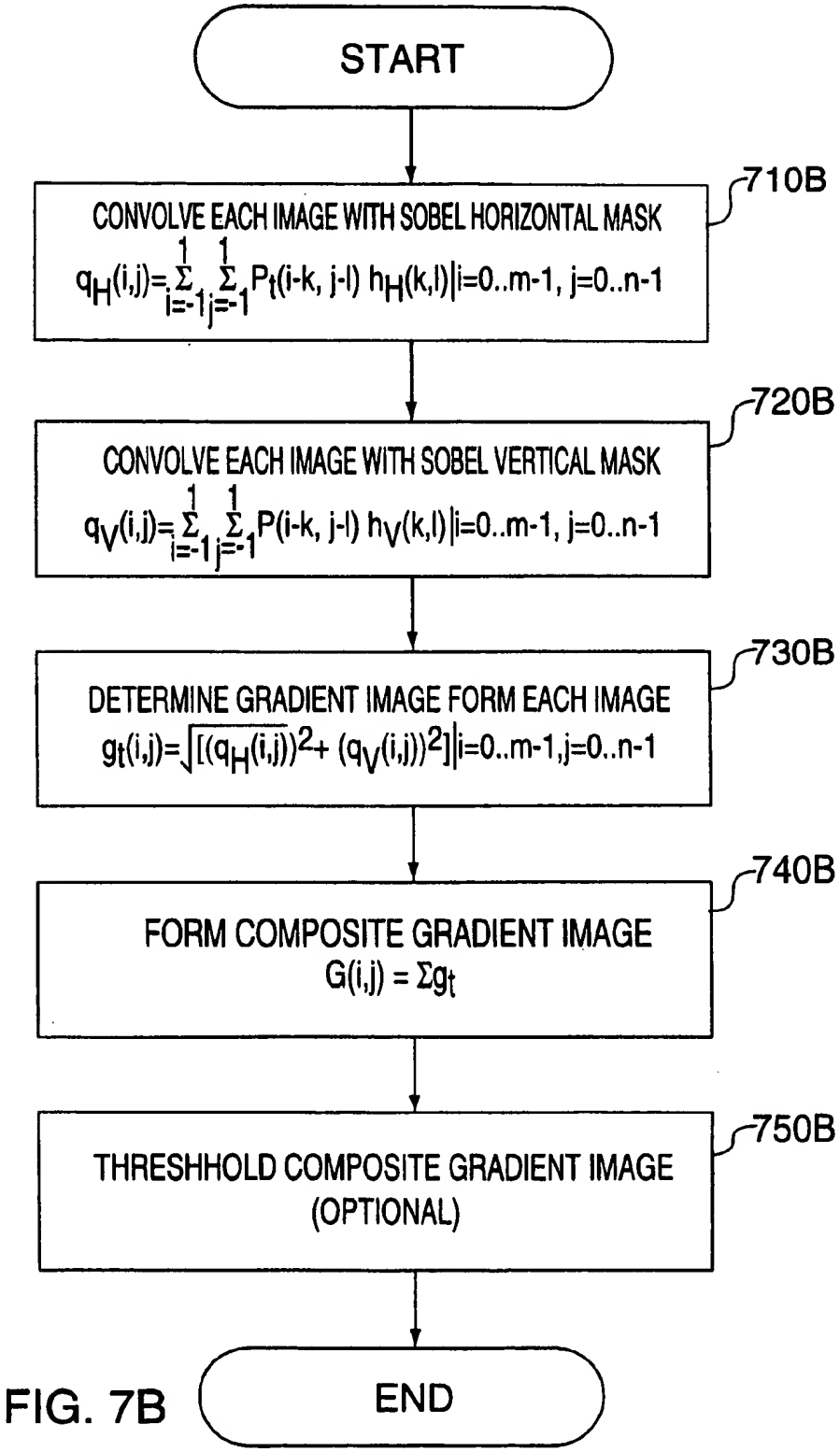

START
710B
CONVOLVE EACH IMAGE WITH SOBEL HORIZONTAL MASK
$q_H(i,j)=\sum_{i=-1}^{1}\sum_{j=-1}^{1}P_t(i-k, j-l)\, h_H(k,l) \mid i=0..m-1, j=0..n-1$
720B
CONVOLVE EACH IMAGE WITH SOBEL VERTICAL MASK
$q_V(i,j)=\sum_{i=-1}^{1}\sum_{j=-1}^{1}P(i-k, j-l)\, h_V(k,l) \mid i=0..m-1, j=0..n-1$
730B
DETERMINE GRADIENT IMAGE FORM EACH IMAGE
$g_t(i,j)=\sqrt{[(q_H(i,j))^2+ (q_V(i,j))^2]} \mid i=0..m-1, j=0..n-1$
740B
FORM COMPOSITE GRADIENT IMAGE
$G(i,j) = \Sigma g_t$
750B
THRESHHOLD COMPOSITE GRADIENT IMAGE
(OPTIONAL)
END

FIG. 7B

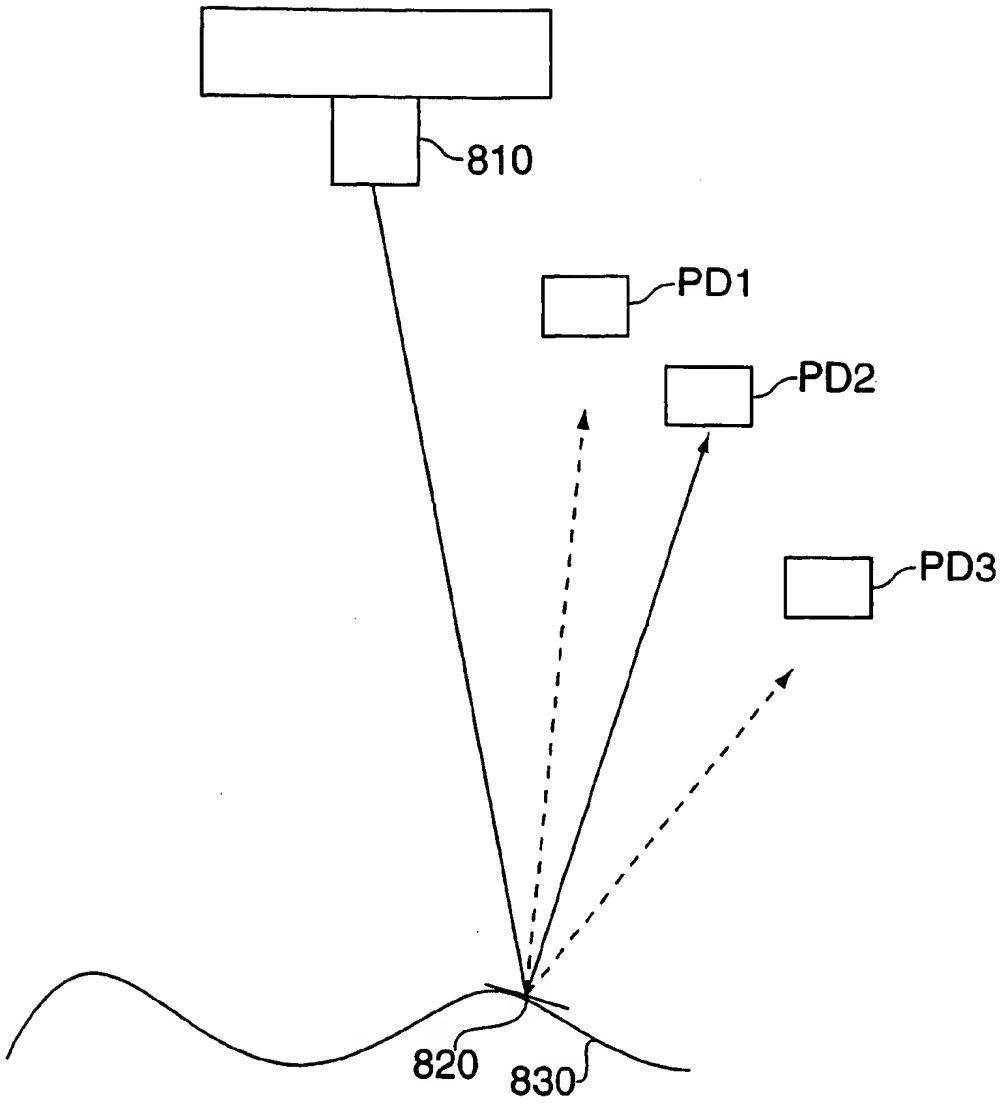


FIG. 8

1	1	1	1	1	0	0	0	1	1	1	1	0	0	0	1	1	0	0	0
1	1	1	1	1	0	0	0	1	1	1	1	0	0	0	1	1	0	0	0
1	1	1	1	1	0	0	0	1	1	1	1	0	0	0	1	1	0	0	0
0	0	0	1	1	0	0	0	1	1	1	1	0	0	0	1	1	1	1	0
0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1
0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	0	0	1	1	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1
1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1
0	0	0	0	1	1	0	0	1	1	1	0	0	0	1	1	1	1	1	1
0	0	0	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0

FIG. 9

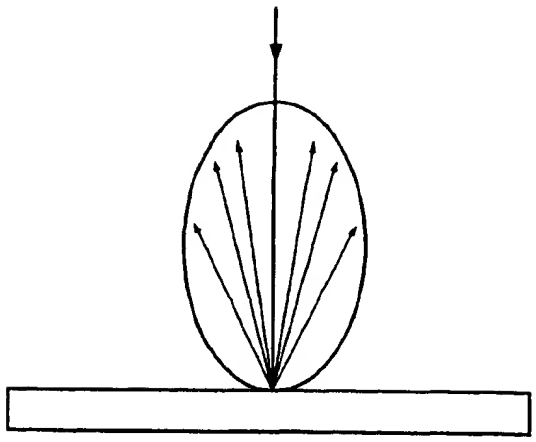


FIG. 10A

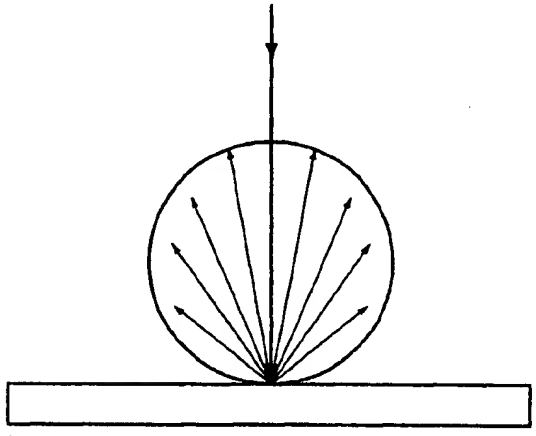


FIG. 10B

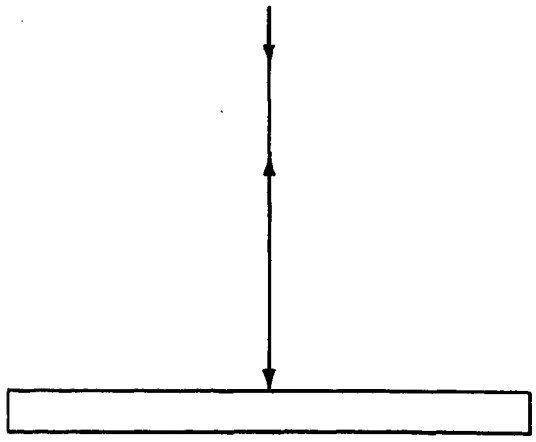


FIG. 10C

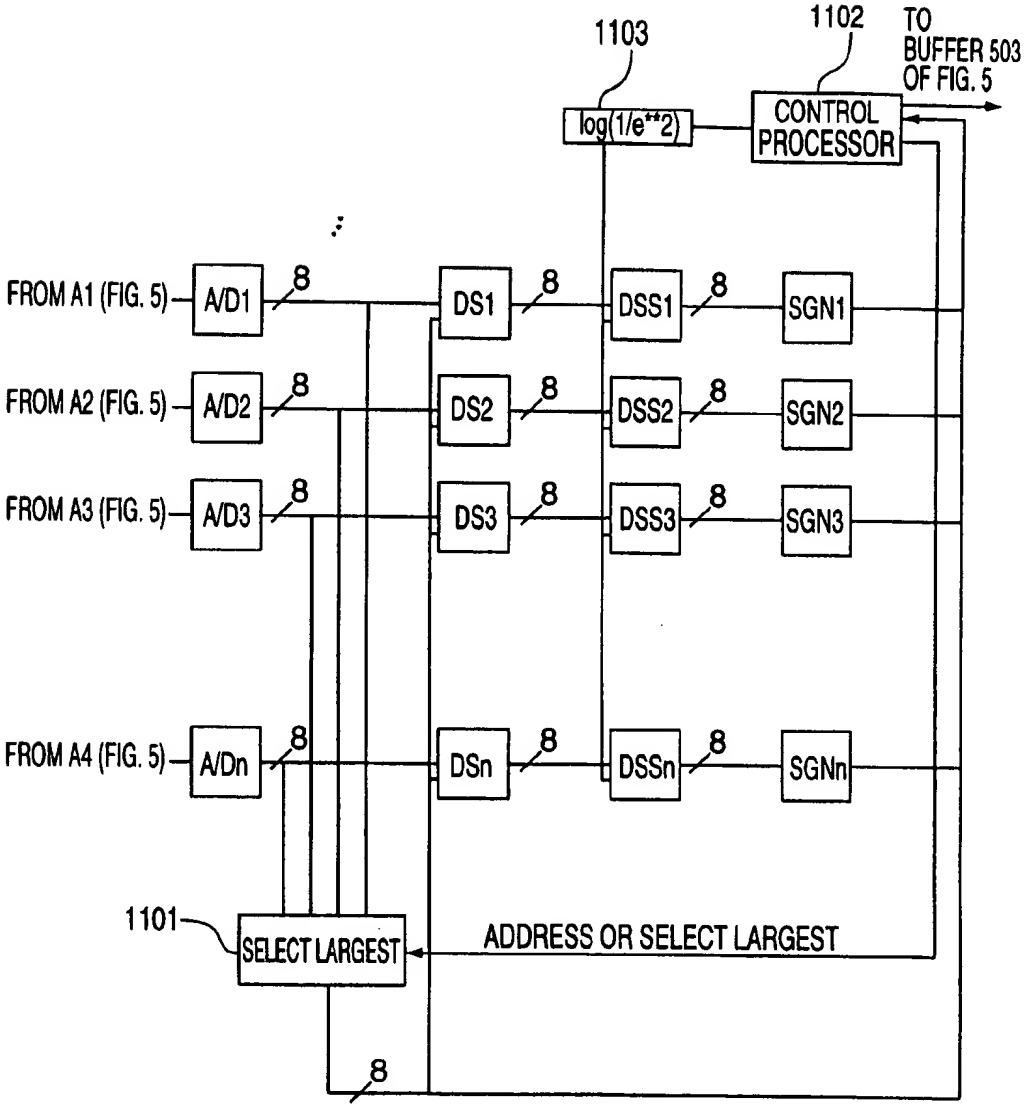

1103
1102
TO BUFFER 503 OF FIG. 5
log(1/e**2)
CONTROL PROCESSOR
FROM A1 (FIG. 5)
A/D1
DS1
DSS1
SGN1
FROM A2 (FIG. 5)
A/D2
DS2
DSS2
SGN2
FROM A3 (FIG. 5)
A/D3
DS3
DSS3
SGN3
FROM A4 (FIG. 5)
A/Dn
DSn
DSSn
SGNn
8
1101
SELECT LARGEST
ADDRESS OR SELECT LARGEST

FIG. 11

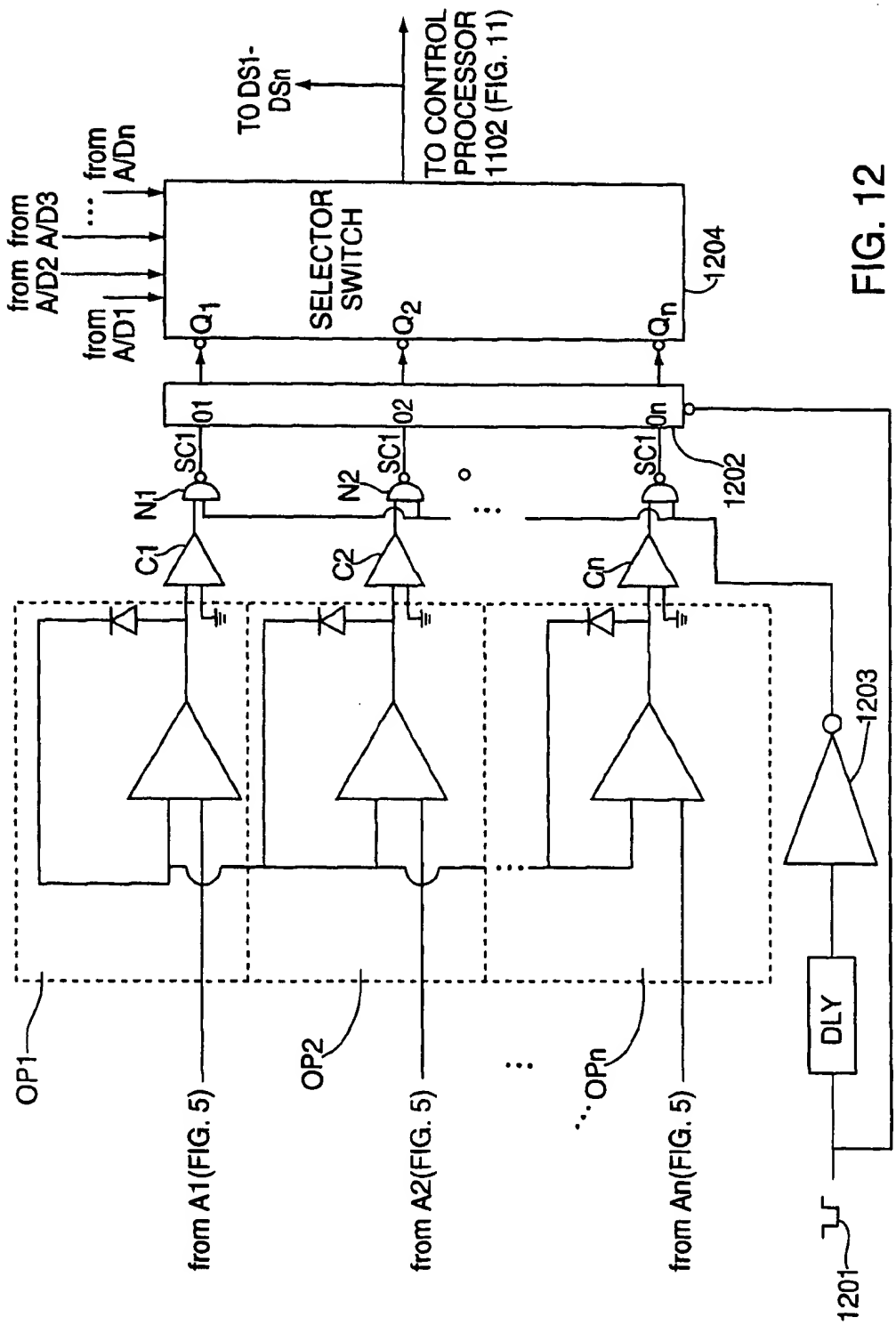

TO DS1-DSn
TO CONTROL PROCESSOR 1102 (FIG. 11)
from A/Dn
from from A/D3 A/D2
from A/D1
SELECTOR SWITCH
1204
Q1
Q2
Qn
01
02
On
SC1
N1
N2
C1
C2
Cn
1202
1203
DLY
OP1
OP2
OPn
from A1(FIG. 5)
from A2(FIG. 5)
from An(FIG. 5)
1201

FIG. 12

METHOD AND SYSTEM FOR IMAGING AN OBJECT OR PATTERN

This is a division of application Ser. No. 08/748,040, filed Nov. 12, 1996.

FIELD OF INVENTION

The present invention is directed to a system and method for imaging objects or patterns. More particularly, the present invention is directed to a system and method for simultaneously obtaining a plurality of images of an object or pattern from a plurality of different viewpoints.

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BACKGROUND IN THE INVENTION

Machine vision systems are commonly used in industry for high speed inspections. In particular, these systems are used to obtain digital images of objects in order to determine, with a computer, whether the object is of "acceptable" quality with respect to predetermined specifications. For example, a system may inspect a semiconductor chip package to determine whether each of the leads of the package have the proper dimensions. A system may also inspect for coplanarity of solder balls on ball grid arrays.

Patterns such as bar codes and data codes are also imaged by such systems. Images of these patterns are analyzed by a computer and in order to "read" the information represented by these codes.

In a machine vision system, an object (or pattern) is typically imaged by illuminating the object with light sources and capturing the light reflected from the object with a video camera (i.e., a photodetector). A digital image is formed from the image received by the camera and the digital data is analyzed by a computer in order to determine characteristics of the object or pattern.

Obtaining a proper contrast between the object or pattern and the background is critical to obtaining an image of sufficient clarity for accurate analysis by a computer. In current practice, an engineer or knowledgeable user obtains the proper contrast by varying the positions of the light sources with respect to the object or pattern being viewed and with respect to the video camera recording the scene. Additionally, the intensity and possibly the polarization and color of the light sources are varied. To achieve the desired contrast, the illumination is often manipulated to make the background either dark with respect to the object features or pattern (dark-field illumination) or bright with respect to the object features or pattern (bright-field illumination). Obtaining the proper illumination is particularly difficult when working with specular (mirror-like) surfaces, especially when the specular surfaces are curved or multifaceted.

One technique for illuminating an object for imaging purposes is described in U.S. Pat. No. 5,461,417 issued to White et al. (the "White '417" patent), expressly incorporated herein by reference. The White '417 patent discloses a system for providing a continuous, uniform, diffuse lighting environment. This system is satisfactory for certain types of

applications. Another technique for illumination is described in U.S. Pat. No. 5,187,611 issued to White et al., expressly incorporated herein by reference. In this patent, a Diffuse On-Axis Light (DOAL) is described which is also beneficial in certain applications. However, good contrast sometimes requires edges to be highlighted which is best obtained from collimated unidirectional light, not uniformly diffuse light.

For certain objects, it may be advantageous to sequentially illuminate an object from a number of different viewpoints and take a picture of the object for each illumination. The pictures can then be combined into a single image. Such a system is described in U.S. Pat. No. 5,060,065 issued to Wasserman, expressly incorporated herein by reference. It may be desirable, for example, to image an object using a bright-field illumination method and subsequently image the same object using a dark-field illumination method. The bright-field and dark-field images can then be individually analyzed or can be first combined, and then analyzed.

Unfortunately, the sequential illumination method increases capture time since a separate picture is required for each illumination—each video picture typically requires 1/30 second. Thus, if lights at three different locations from the object are utilized, three pictures would be required.

Furthermore, the combined image tends to look smeared if there is any relative motion between the object and the camera. For example, vibration may cause the object to move slightly. Since an image of the object before the motion and after the motion will not exactly coincide, the combined image will appear smeared.

SUMMARY OF THE INVENTION

The present invention provides a system and method for simultaneously obtaining a plurality of images of an object or pattern from a plurality of different viewpoints. In an exemplary embodiment of the invention, proper image contrast is obtained by replacing the light sources of earlier systems with equivalent light sensitive devices and replacing the cameras of earlier systems with equivalent light sources. With such a system, bright-field images and dark-field images may be simultaneously obtained.

In one aspect of the invention, a light source is positioned to illuminate at least a portion of an object.

A plurality of light guides having input ends are positioned to simultaneously receive light reflected from the object and transmit the received light to a plurality of photodetectors. The light guides are arranged such that their respective input ends are spaced substantially equally along at least a portion of a surface of an imaginary hemisphere surrounding the object. The signals generated by the photodetectors (as a result of light detection) are processed and a plurality of images of the object are formed.

Another aspect of the invention provides a method for generating composite images from simultaneously obtained images. Equivalent regions of each image (corresponding to geographically identical subpictures) are compared. The subpicture having the highest entropy is selected and stored. This process continues until all subpictures have been considered. A new composite picture is generated by pasting together the selected subpictures.

In another aspect of the invention, the vector of relative light values gathered for each pixel or region of an object illuminated or scanned (i.e., one value for each photodetector) is used to determine reflectance properties of points or regions illuminated on the object or pattern. The reflectance properties may be stored in a matrix and the matrix used to read, for example, a Bar Code.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other features of the present invention will be more readily apparent from the following detailed description of exemplary embodiments taken in conjunction with the attached drawings wherein:

FIG. **1A** is a diagram of a bright-field illumination system;

FIG. **1B** is an illustration of an image obtained using the bright-field method of illumination;

FIG. **2A** is a diagram of a dark-field illumination system;

FIG. **2B** is an illustration of an image obtained using the dark-field method of illumination;

FIG. **3** illustrates a sequential illumination system;

FIG. **4A** is a diagram of an exemplary system illustrating the principles of the present invention;

FIG. **4B** is a diagram of an exemplary photodetector arrangement;

FIG. **4C** is a diagram of a sequential illumination system for reading characters;

FIG. **4D** is a diagram of an:exemplary system in accordance with the principles of the,present invention corresponding to FIG. **4C**;

FIG. **5** illustrates the principles of the present invention in further detail;

FIG. **6** illustrates the scanner and photodiode arrangement of FIG. **5** in further detail;

FIG. **7A** is a flowchart of an illustrative process for patching an image;

FIG. **7B** is a flowchart illustrating composite gradiant image generation;

FIG. **8** illustrates a scanner illuminating a point on a surface;

FIG. **9** illustrates a matrix representing reflectance properties of a 2-D Bar Code;

FIG. **10A** illustrates reflecting properties of a shiny surface;

FIG. **10B** illustrates reflecting properties of a diffuse surface;

FIG. **10C** illustrates reflecting properties of a mirror (specular) surface;

FIG. **11** is a diagram of an exemplary embodiment of pre-processing hardware; and

FIG. **12** is a diagram of an enhancement to FIG. **11**.

DETAILED DESCRIPTION

Bright-field Illumination

Referring now to the drawings, and initially FIG. **1A**, there is illustrated a simple bright-field illumination system **100**. A video camera **110** having a lens **115** is positioned to image a shiny plate **120** having a diffuse (Lambertian) gray circle **125** painted on it. The reflecting properties of shiny, diffuse, and mirror (specular) surfaces are shown in FIGS. **10A**, **10B**, and **10C** respectively. The shiny plate **120** is orthogonal to the viewing axis of the camera **110**. Two light sources ("upper light sources") **130** and **135**, positioned equi-distantly from the shiny plate **120** and in close proximity to the camera lens **115**, illuminate the shiny plate **120** and gray circle **125**. The shiny plate **120** reflects light directly back to the camera **110**. The circle **125**, since it is diffuse, scatters the light **150**. FIG. **1B** illustrates the bright-field image formed by the camera **110**. As shown, the image of the circle **125B** appears dark relative to the bright background **120B**. If the shiny plate is replaced with a true mirror, beam splitter **160** and lamp **170** would be required to direct the light parallel to the camera axis to obtain true bright-field illumination.

Dark-field Illumination

FIG. **2A** illustrates a dark-field illumination system. In this system, a camera **210**, lens **215**, and shiny plate **220** with a gray circle **225** are positioned in the same manner as in FIG. 1A. Here, however, light sources ("lower light sources") **260** and **265** are each positioned off to the side (with respect to the camera **210** field of view) and close to the shiny plate **220**. The light sources **260** and **265** are also positioned approximately equi-distantly from the shiny plate **220**. Light shrouds **275** prevent light from passing directly from lamps **260** and **265** to lens **215**. Light emanating from the light sources **260** and **265** is reflected as light **270** by the shiny plate **220** in a direction away from the camera lens **215**. Light impinging on the gray circle **225** is scattered. As illustrated, at least some light (**280**) of the light impinging on the gray circle **225** is reflected toward the camera lens **215**. FIG. **2B** illustrates the dark-field image captured by the camera **210**. Here, the image of the circle **225B** appears bright relative to the dark background **220B**.

Combined System

In both the bright-field illumination system and the dark-field illumination system, if the shiny surface (in FIGS. **1A** and **2A**) is not perfectly flat, other bright and dark regions may appear in the image background. For example, the surface may reflect in such a way to create both real and virtual images, each of which is imaged by the video camera. Thus, it may be desirable to illuminate an object from two or more different angles (with respect to the object). Accordingly, as illustrated in FIG. **3**, a single system may include upper light sources **330** and **335** (corresponding to light sources **130** and **135** of FIG. **1A**) and lower light sources **360** and **365** (corresponding to light sources **260** and **265** of FIG. **2A**). Each set of light sources (i.e., upper light sources **330** and **335**, and lower light sources **360** and **365**) may be independently used to illuminate the object (here, shiny plate **320** with gray circle **325**), with an image being captured by the video camera **310** for each. The most "useful" portions of the bright-field image and the dark-field image captured can be analyzed independently or can be combined to provide a single image of the object.

Points on some surfaces have complex reflectance properties that are combinations of those shown in FIGS. **10A**, **10B**, and **10C**. Also, there may be surface regions viewed by the system of FIG. **3** that are curved or tilted with respect to the horizontal, which may spoil the bright-field or dark-field views. Therefore, the system of FIG. **3** may not satisfy a wide range of conditions that include unusual reflectance characteristics, or curved, or multi-sloped surfaces.

As noted above, this sequential illumination method increases capture time since a picture, e.g., a video frame, is required for each illumination. Furthermore, the combined image will appear smeared if there is any relative movement between the camera and the object.

Exemplary Embodiment

The present invention solves many imaging problems by simultaneously obtaining a plurality of images of the object. Specifically, the present invention provides the proper "contrast" by replacing the light sources of earlier systems with equivalent "cameras" and the cameras of the earlier systems with equivalent light sources. With such a system, a wide choice of illumination viewpoints may be obtained to obtain bright-field or dark-field images regardless of the exact local surface properties or orientation of the object or pattern being viewed.

An exemplary system implementing the principles of the present invention is illustrated in FIG. **4A**. A scanner **410** is

positioned to illuminate a shiny plate **420** having a diffuse gray circle **425** painted on it. The scanner **410**, which has a light beam that may be, for example, continuous or AC or pulse modulated, generates a raster scanned light spot that scans across the object but emanates from the location previously occupied by the camera lens **315** of FIG. **3**. The light spot may be "white" or a single color as is generated, for example, by a light emitting diode (LED). Alternatively, the light spot may be a single wavelength as may be generated by a laser.

As illustrated in FIG. **4A**, the light sources of FIG. **3**, i.e., **330**, **335**, **360**, and **365**, are replaced with photodetectors **430**, **435**, **460**, and **465** such as, for example, photodiode pickups. Because the light spot is scanned in a raster pattern, each of the photodetectors **430**, **435**, **460**, and **465** generates a "video" signal that is synchronized with all other photodetectors **430**, **435**, **460**, and **465**. That is, at each instant of time, the signal generated at each photodetector **430**, **435**, **460**, and **465** is as a result of the illumination of the same "pixel" (light spot on a small region of the object). However, the signals generated at each photodetector **430**, **435**, **460**, and **465** vary in amplitude according to the reflectance properties and orientation of the area being illuminated with respect to the relative position of the scanner **410** and the photodetector **430**, **435**, **460**, and **465**.

Due to the reversibility of light rays, a region of the object (i.e., the shiny plate **420**) that would appear bright to the camera **310** of FIG. **3** when illuminated by a particular light source, will generate a strong signal when illuminated with a light source (i.e., scanner **410**) at the position of the original camera, but sensed by a photodetector at the location of the original light source. Similarly, a region that appeared to be dim to the camera **310** of FIG. **3** when illuminated by a particular light source will generate a weak signal when illuminated with a light source (scanner **310**) at the position of the original camera **310** of FIG. **3**, but sensed by a light sensor at the location of the original light source. Thus, when the background of the shiny plate **420** is illuminated by the scanner **410**, photodetectors **430** and **435** generate a relatively strong signal while photodetectors **460** and **465** generate a relatively weak signal. Furthermore, when the gray diffuse circle **425** is illuminated by the scanner **410**, photodetectors **430** and **435** generate a relatively weak signal while photodetectors **460** and **465** generate relatively strong signals. Accordingly, photodetectors **430** and **435** capture bright-field images of the shiny plate **420** while photodetector **460** and **465** capture dark-field images of the shiny plate **420**.

Applying the principles of the present invention, many equivalent "illumination viewpoints" can be simultaneously captured by strategically positioning simple light pickups such as, for example, photodiodes at viewpoints surrounding the object to be viewed. Accordingly, bright-field images and dark-field images from different viewpoints can simultaneously be captured.

In accordance with the principles of the present invention, the light sensitive devices of the illustrated embodiments may employ lenses, fiber optics, light guides, or simple photodetectors. The photodetectors may be photomultipliers or semiconductor photodiodes such as, for example, avalanche photodiodes, or phototransistors.

Furthermore, multiple photodetectors can be arranged at a particular viewpoint to replace or correspond to different types of light sources. Referring to FIG. **4B**, an exemplary photodetector arrangement is illustrated, generally corresponding to an array of lensed LEDs used in many machine vision applications. Each lens **410B** of a lenslet array **420B** focusses light onto a corresponding photodiode **430B** of a photodiode array **440B**. The output signal from each photodiode **430B** is applied to a summing amplifier **450B**. The output signal from the summing amplifier **450B** may then be sampled. In another embodiment, the output signal from each individual photodiode **450B** may be individually sampled. The arrangement of FIG. **4B** is particularly suitable for viewing certain specular surfaces which are normally best viewed with distributed light sources. As an alternative, a single fiber bundle or light guide may be used to gather the light from each lenslet at its focal point, and the light from all of the bundles or light guides may be summed at a single photodetector.

In applying the principles of the present invention, a major benefit is that commercially available machine vision system optics or fiber optics may be utilized. For example, Fiber-Lite®, manufactured by Dolan-Jenner Industries, is an illumination system that couples a light input through a fiber optic assembly to form a line of light (MV-IND150LA), an area of light (MV-IND150ABL), a point of light (MV-IND150FO), or a ring of light (MV-IND150RL). Any of these assemblies can be used to create a correspondingly shaped "equivalent" to the light source by replacing the light normally used as input to the fiber optic assembly with a photodetector apparatus that provides the desired output signals.

APPLICATION OF THE PRINCIPLES OF THE PRESENT INVENTION

When imaging characters (e.g., serial numbers) that are positioned on a semiconductor wafer, prior art systems typically require that light sources be located at a particular critical location according to the reflectance properties of both the wafer and the characters on the wafer. However, both surface and sub-surface properties may change depending on where in the semiconductor manufacturing process (i.e., what process step) the characters are being imaged. With prior art systems, many illumination locations may have to be tested before the characters can be properly read. An example of various type of illumination that could be used for imaging characters on a wafer using standard machine vision techniques is shown in FIG. **4C**. As illustrated, characters on wafer **400C** are sequentially illuminated by a high dark field light source **410C**, (used to produce a dark-field image), a high DOAL (diffuse on axis light) **420C** (positioned to produce a bright-field image), and a low DOAL **430C** (positioned to produce a bright-field image). A camera **450C** must capture three separate images of the characters—one per light source.

Referring now to FIG. **4D**, in accordance with the principles of the present invention, each of the light sources (i.e., **410C**, **420C**, and **430C**) are replaced with a corresponding photodetector (**410D**, **420D**, and **430D**) while the camera **450B** is replaced with a laser scanner (**450C**). Here, the characters on the wafer are required to be scanned only one time, with three images being simultaneously captured by the photodetectors **410D**, **420D**, and **430D**.

Detailed Diagram

FIG. **5** is a diagram illustrating the general principles of the present invention in further detail. A scanner **500**, positioned to illuminate an object **501** (such as, for example, a semiconductor package), is controlled by scan control circuitry **502** (under the control of sync signals from a microprocessor or associated hardware **503**) to scan the object **501** in a raster pattern. Specifically, the scan control circuitry **501** provides horizontal and vertical scan control signals **504** and a pixel clock signal **505**, to control the

scanner **500** to sequentially illuminate each spot (i.e., pixel) on the object **501**.

Photodetectors, for example, photodiodes PD1–PDn, are positioned to capture light reflected by the object **501** (as a result of illumination by the scanner **500**) from various viewpoints. As illustrated, for a horizontal surface, the photodiodes positioned closest to the object **501** (i.e., photodiodes PD5–PDn) provide dark-field images while the remaining photodiodes (i.e., PD1–PD4) are positioned for bright-field imaging. However, when imaging a portion of a specular surface that is at a steep angle to the horizontal, the roles of the PD1–PD4 and PD5–PDn may reverse in which case PD5–PDn would provide bright-field images and PD1–PD4 would provide dark-field images. Depending on the complexity of the surfaces being imaged, more or less photodiodes than are shown in FIG. **5** may be used to gather sufficient data for a particular machine vision application.

Each of the photodiodes PD1–PDn is connected to an amplifier A1–An for amplifying the signals (representing the intensity of the reflected light detected by the photodiodes PD1–PDn) generated by the photodiodes PD1–PDn. Due to the variation in specularity of the surfaces of the scanned object **501**, light intensity levels into the photodiodes PD1–PDn may have a very large dynamic range. Accordingly, logarithmic amplifiers may be advantageously used. In the exemplary embodiment of the present invention, although other amplifiers may be used, logarithmic amplifiers provide several advantages over linear amplifiers (although other types of amplifiers may be used):

- the logarithmic output signal is compressed so that fewer bits are needed to represent the signal—in spite of the large dynamic range;
- logarithmic output signals are easily processed when looking for significant changes (edges) since the same percentage change in a signal always corresponds to the same numeric difference regardless of the signal amplitude; and
- logarithmic output signals may be easily normalized since dividing the output signal by a reference signal is performed by simply subtracting the reference from the output.

Each of the amplifiers A1–An is connected to a sample and hold circuit (or register) SH1–SHn for sampling the signals output by the amplifiers A1–An. The sample and hold circuits SH1–SHn are synchronized with the scanner by scan control circuitry **502** so that signals representing the intensity of reflected light detected by photo detectors PD1–PDn at the same given instant in time are sampled for each spot of the object illuminated by the scanner **500**. The signals output by the sample and hold circuitry SH1–SHn are applied to a multiplexer MPX. Under the control of data control circuitry **506** (which is, in turn, controlled by the microprocessor) the analog signals from the sample and hold circuitry SH1–SHn are sequentially applied to an analog to digital (A/D) converter **507** by the multiplexer MPX. The digital signals generated by the A/D converter **507** are buffered in a buffer memory **508** (or other recording device) at addresses identified by the data control circuitry **507** (under the control of the microprocessor **503**).

In operation, each spot illuminated by the scanner **500** is simultaneously imaged by the photodiodes PD1–PDn. That is, for each spot illuminated at a given X-Y coordinate, a digital intensity value is stored in the buffer memory **508** representing the intensity of the light reflected by the object **501** as detected by each of the photodiodes PD1–PDn. Accordingly, for the exemplary embodiment of the present invention, n images of the object **501** are captured (i.e., one image per photodiode) as a result of a single scan of the object **501**.

FIG. **6** illustrates the scanner **500** and the photodiode PD1–PDn arrangement in further detail. A light beam **600** from a light source **610**, such as, for example a commercially available collimated laser diode light source, is directed though a beam splitter **620** into a lens **630** that focusses the beam **600** to a predetermined spot size on plane **660** via X and Y mirror galvanometers **640** and **650**. The X galvanometer **640**, controlled by the X and Y scan control signals **504** of FIG. **5** and preferably oscillating in accordance with pixel clock **505**, reflects the beam **600** onto a Y mirror galvanometer **650**. The Y galvanometer **650**, also controlled by the X and Y scan control signals **504**, reflects the beam **600** onto a point of the object **660** under examination. As will be understood by those of skill in the art, sequentially moving the X galvanometer **640** in the direction of arrow **640A** causes the beam **600** to illuminate points on the object's surface along an X axis, while sequentially moving the Y galvanometer **650** in the direction of arrow **650A** causes the beam **600** to illuminate points along a Y axis. Accordingly, the scanner **500** is controllable to illuminate each point on the object's surface **660** in a raster pattern. This spot may be illuminated continuously or just during a brief interval at each pixel position as it travels from one pixel position to another according to the pixel clock signal **505**.

In another embodiment, the X galvanometer **640** may be replaced with a fixed mirror so that the object **660** is scanned in a single line along the Y axis. The object **660** may then be translated in the X direction via a conveyor or translation table in order to raster scan the object **660**. Similarly, the Y galvanometer **650** may be replaced with a fixed mirror and the object **660** translated in the Y direction, or both galvanometers **640** and **650** may be replaced with fixed mirrors and the object translated by an X-Y translation table.

Furthermore, although galvanometers **650** and **660** are shown, other deflection devices such as rotating polygons with mirrored surfaces, rotating prisms, and acousto-optic beam deflectors, all of which are well known in the art, may be used to obtain the desired scan pattern. Also, the light beam deflection optics may have many variants such as the use of potical scan lenses **680** (for example, an F-Theta or telecentric lens) between the last beam deflector (here, galvanometer **650**) and the object which can be used to provide a more uniform scan pattern or a pattern in which the beam remains substantially perpendicular to surface **660** over all X,Y beam positions.

As shown in FIG. **6**, the scanner **500** of the exemplary embodiment further includes a lens **670** which focusses light reflected from the object along the beam path **600** onto a photodiode PDn+1 to sample the light that returns directly along the illumination path. This photodiode corresponds to light source **170** of FIG. **1A**. Also, a stop **671** is included to absorb light that is deflected by beam splitter **620**.

In the exemplary embodiment of the present invention, light guides LG1–LGn are distributed around the periphery of an imaginary hemisphere surrounding the object such that their respective input ends are uniformly angularly spaced when viewed from the center of the hemisphere (i.e., the approximate object location). Simple patterns such as closely packed circles or hexagons may be used to evenly space the input ends of the light guides LG1–LGn in azimuth and elevation along the entire surface of the hemisphere, each of the ends in a center of a circle or hexagon. In the exemplary embodiment, if hexagons are used, the axis of the center beam from scanner **500** may be aligned with a corner where three hexagons meet. Alternatively, the axis of the center ray beam of the scanner **500** may be aligned with the center of the "top" hexagon. Many other distribution schemes are possible.

In the exemplary embodiment, each of the individual light guide LG1–LGn input ends may lie above or below the surface of the hemisphere. However, each light guide LG1–LGn input end is positioned to maintain the desired angular location when viewed from the object. Output variations between the photodetectors that are connected to light guides LG1–LGn whose input ends are closer or further to the object may be removed during equipment calibration or via computation. Computations are based on the known distance between each input end and the normal object location using the inverse square law.

The output ends of the light guides LG1–LGn are proximity focused onto associated photodetectors, i.e., photodiodes PD1–PDn (described above in connection with FIG. **5**).

In an alternative embodiment, a separate lens may be used to image the output end of each light guide LG1–LGn onto its corresponding photodiode PD1–PDn.

Also, a separate lens may be used to image the field of view onto each light guide input end. When such is the case, the separate lens may be selected with a large numerical aperture for maximum light capture. Depth of field and exact focus are not as important considerations as they would be in a camera lens which must resolve adjacent pixels. If the lens associated with the input end of the fiber is somewhat out of focus so that light spills outside of the fiber end, it merely reduces the amount of light captured—it down not affect the sharpness of the captured image. Conversely, depth of field and focus is an important issue for the raster scanned beam. If this beam is out of exact focus or if the scene being scanned does not fall into the depth of field of the scanning beam, the captured image will be blurred since the light spot impinging on the surface being scanned may be significantly larger than the space between pixels as defined by the distance between illuminating pulses or recording intervals. Maximizing the depth of field requires minimizing the numerical aperture of the spot scanner optics, which makes it important to choose a bright source if it is desired to maintain a high level of illumination. When the brightest spot is desired, a laser is a suitable light source. When using a laser for illumination, it is also possible to use narrow bandpass light filters (for example, of 10 nm width) to eliminate ambient light while passing scanned light reflected from the scene into the phtodetectors. Such filters may be placed anywhere in the light path between the scene and the photodetectors.

In accordance with the exemplary embodiment, when substituting photodetectors for a light source at a particular viewpoint as described in connection with FIGS. **4A**, **5**, and **6**, several factors may be taken into account, such as, for example, sensitivity at chosen wavelengths, dynamic range, and frequency response. Avalanche photodiodes are generally very fast devices with large dynamic ranges and are particularly well suited for capturing high speed pulses at extremely low light levels due to their very high sensitivity. Photomultipliers have similar properties.

The ordinary photodiode, p-i-n photodiode, or phototransistor is also capable of good performance in video application but is of less utility with extremely high speed pulses at extremely low light levels. All of the solid state photodetector devices lose their high frequency capability as their area (and hence capacitance) increases. Accordingly, although it would appear easiest to emulate a light source viewpoint by locating the photosensitive device at the desired position and enlarging its area until it equaled that of the light source it was replacing, the loss of high frequency response and increase in attendant noise (due to increased area) will not always permit this approach.

One exemplary approach, however, is to use a lens to image the scanned scene onto the photosensitive device. This increases the energy collected to that collected over the area of the lens without increasing the area of the photodetector (with all of the corresponding disadvantages). Alternatively, in some applications, a non-imaging device, such as, for example, a tapered light pipe, may be used instead of a lens. With certain limits, the gain achieved via a tapered light pipe is equal to the input area divided by the area exiting to the photodetector. If an attempt is made to achieve too high a gain, the output rays will emerge almost parallel to the photodetector surface, and by Fresnel relationships, be reflected by the photodetector rather than absorbed.

Calibration

The exemplary embodiment illustrated in FIGS. **5** and **6** may be calibrated by scanning a flat white object and normalizing the output from each photodiode PD1–PDn with respect to each other. The correction values for normalization may then be stored in a table in memory accessible by microprocessor **503**, and used during image processing. Although one value could be recorded for each illuminated position of the raster scan, it may only be necessary to store a small subset of this information since the correction values will generally vary very slowly across the field of view.

Composite Images

When a specular object has a curved or multi-faceted surface, there may be no individual image captured that has useful data that covers the entire object. In such a case, it may be necessary for the microprocessor **503** to patch together the "best" portions (i.e., the portions having the highest information content) of each of the pictures obtained from each viewpoint to form a composite image. The flowchart of FIG. **7A** shows an exemplary process performed by the microprocessor **503** for "patching" an image.

In accordance with the exemplary process, equivalent regions of each image (corresponding to geographically identical subpictures) are compared(step **710**). Since the "useful" portion of a scene will generally be the portion with the highest entropy—in a practical sense, the portion with the most change or "detail," the subpicture having the highest entropy (for the image information sought) is selected and is stored in memory (step **720**).

One way to determine the entropy of each subpicture is to pass each subpicture through a 2-D high-pass spatial frequency filter and then square each resulting pixel value. If desired, each pixel may be compared to a threshold value and set to zero if less than the threshold value (in order to eliminate pixels representing noise). The pixel values in the subpicture may then be summed to obtain a value for the entropy of the subpicture.

When certain characteristics of the subpicture desired are known in advance, such as the particular frequency or pitch that may be present in the image of a 2-D bar code, the subpicture may be passed through a corresponding bandpass spatial filter in place of, or in addition to, the aforementioned high-pass filter.

This process of FIG. **7A** continues until all subpictures have been considered (step **730**). A new composite picture is then generated (by patching together the selected subpictures) (step **740**) that best expresses the detail or structure of the pattern or object being examined.

In the exemplary embodiment, patching is simple because there is no perspective distortion due to the varied viewpoints. Data captured at the same instant of time at each viewpoint will almost always be from the same illuminated

spot or "pixel." Occasionally light may be received via a multiple reflection, but this will not be the usual case.

As one of skill in the art will understand, however, it may be necessary to conform the selected subpictures to each other. For example, assume that images are represented by N×M bit matrices wherein a "1" represents bright and a "0" represents dark. If a bright field subpicture and a dark-field subpicture are to be patched together, each bit in one of the subpictures, for example, the dark-field subpicture, is XOR'ed with a "1" so as to "flip the bits" of the subpicture to conform it to the bright-field subpicture. In effect, the dark-field subpicture is converted to an equivalent bright-field subpicture. Of course, the bright-field subpicture may be converted to an equivalent dark-field subpicture in a similar manner.

Although the composite image obtained as described in connection with FIG. 7A may be processed to reveal edges, a composite edge image or composite gradient magnitude image may also be derived directly from the individual images obtained from each of the photodetectors.

FIG. 7B is a flowchart of an exemplary process for deriving the composite gradient magnitude image directly from the individual images. Gradient magnitude is computed as follows:

$$df/dr=\sqrt{[(df/dx)^2+(df/dy)^2]}\,|\,i=0\ldots m-1,\ j=0\ldots n-1$$

Accordingly, in step **710B**, df/dx is derived (for each of the image matrices P_1–P_s obtained from the photodetectors) from the convolution of each image matrix P_1–P_s with the Sobel horizontal mask h_H (i.e., the Sobel kernal sensitive to vertical edges):

$$h_H=\begin{bmatrix}1 & 0 & -1\\ 2 & 0 & -2\\ 1 & 0 & -1\end{bmatrix}.$$

Thus,

$$q_h(i,j)=\sum_{i=-1}^{1}\sum_{j=-1}^{1}P_t(i-k,j-1)h_H(k,1)\,|\,i=0\cdots m-1,\ j=0\cdots n-1$$

is calculated for each image matrix (step **710B**).

Next, in step **720B**, df/dy is derived for each of the image matrices P from the convolution of each image matrix P_1–P_s with the Sobel vertical mask h_v (i.e., the Sobel kernal sensitive to horizontal edges):

$$h_v=\begin{bmatrix}-1 & -2 & -1\\ 0 & 0 & 0\\ 1 & 2 & 1\end{bmatrix}.$$

Thus

$$q_v(i,j)=\sum_{i=-1}^{1}\sum_{j=-1}^{1}P_t(i-k,j-1)h_V(k,1)\,|\,i=0\cdots m-1,\ j=0\cdots n-1$$

is calculated for each image matrix (step **720B**).

The discrete gradient at image coordinate i,j is then determined for each image matrix $q_h(i,j)$ as follows:

$$g_t(i,j)=\sqrt{[(q_h(i,j))^2+(q_v(i,j))^2]}\,|\,i=0\ldots m-1,\ j=0\ldots n-1\ \text{(step 730B)}.$$

Finally, the gradient matrices $g_t(i,j)$ corresponding to image matrices P_1–P_s are added together to provide a composite gradient magnitude image matrix G:

$$G(i,j)=\Sigma g_t \qquad \text{(step 740B)}.$$

The composite gradient image may be optionally thresholded (step **750B**).

Reflectance

The vector of relative light values gathered for each pixel or region being illuminated (i.e., one value for each photodiode PD1–PDn of FIG. **5**) provides a means to infer reflectance properties (e.g., the surface is specular or matte) of points or regions illuminated on the object or pattern.

For each vector of relative light values collected for each pixel, for example, the following may be determined by the processor **503** or external circuitry (not shown):

1) the location of the photodetector that has the largest signal and its signal amplitude (the signal amplitude may be used as a reference and the location used to determine the orientation of the point corresponding to the pixel on the object surface);
2) the total (relative) energy received (calculated by, for example, adding together the intensity values represented by each of the signals generated by the photodetectors as a result of detecting light);
3) the median signal amplitude as a fraction of the reference;
4) the mean signal amplitude as a fraction of the reference;
5) the distance from the reference sensor (for a given configuration, the location of each of the sensors is known thus the distance is easily calculated) that must be traveled to obtain a significant fraction of the total energy received (e.g, the fraction of the total number of detectors that capture almost all of the energy)—(this may be calculated, for example, by adding the largest signals—in size order, largest first—until the total is a predetermined percentage of the total energy received by the system and determining how many of signals were added);
6) the standard deviation of the energy received; and
7) the ratio of the largest element of the vector (i.e., the highest light intensity value) to the smallest.

From the above-listed calculations, reflectance properties may be inferred. If, for example, a point on an object is highly specular (in an ideal sense), one photodetector would receive all (or most) of the reflected light energy. As shown in FIG. **8**, for example, a scanner **810** illuminates a point **820** on a surface of an object **830**. If the object is specular at the point **820**, the reflected light intensity detected by one of the photodiodes (in this case, photodiode PD2) will likely be significantly larger than the light detected by neighboring photodiodes (here, photodiodes PD1 and PD3). Similarly, if the vector of light intensity values associated with illumination of the point **820** consists of approximately equal values (except for the cosine falloff with angle), the surface being illuminated is diffuse or matte.

Accordingly, reflectance properties would be evident from all of the values calculated in connection with 1) through 7) above. However, not all values are necessary to infer reflectance properties. For example, the value calculated for item 5, i.e., the fraction of the total number of detectors that capture almost all of the energy, may be sufficient to infer specularity (e.g., item 5 would be very small). Similarly, if the point is completely matte, the computed values corresponding to items 1, 3, and 4 will be close in amplitude. Moreover, the computed values corresponding to items 6 and 7 will be small.

Because reflectance properties corresponding to a point are contained in the computed relationships of the values in

the vector (as set forth, for example, in items 1–7 above), the amount of information that must be stored and processed to sufficiently describe these properties can be significantly decreased. Rather than storing each element of the vector (each element corresponding to one photodetector), it may be only necessary to store a subset of values corresponding to the computed properties of the vector. For example, under certain circumstances, recording items 1, 5, and 6 (above) for each point scanned (as derived from the vector of light intensity values associated with that point) provides sufficient information to infer reflectance. This may be done on a pixel by pixel basis.

In some other circumstances it may only be necessary to store a single bit, a "1" for specular and a "0" for non specular, etc., for each input vector, according to a decision made based on vector data. The data required to be kept will be application specific.

Pre-Processing Circuitry

When a reduction in the amount of data recorded as described above is desired, the input vector must be examined or pre-processed between illumination of adjacent pixels. Accordingly, special purpose hardware can be used to ensure that the required processing can be done in the inter-pixel time interval. Such special purpose processing may take advantage of parallel architecture or mixed analog and digital processing to obtain the necessary speed. The portion of the system outlined in dashed lines **511** illustrated in FIG. **5** may be replaced with such pre-processing hardware.

FIG. **11** illustrates an exemplary embodiment of the pre-processing hardware. As illustrated, the signals from each of the log amplifiers A1–An of FIG. **5** are applied to corresponding analog to digital (A/D) converters A/D1–A/Dn where the analog signals are converted to eight bit digital signals. The digital signals from the A/D converters A/D1–A/Dn (each digital signal representing one vector element) are applied, in parallel to that logic circuit **1101** which identifies and extracts the largest digital signal.

The details of logic circuit **1101** are not shown since there are any number of ways that this can be designed. For example, the most significant bit of each vector element may be examined. Elements having a "0" in this position may be eliminated from further consideration if any of the other elements have a "1" in the same position. This may be repeated for each bit position, one at a time, until the least significant bit of the elements have been considered. At that time, only the largest of the elements will remain. Although this can be performed as a sequential process, it may be advantageous to implement this operation (circuit **1101**) as a parallel process by using hard wired logic (using, for example, a PAL, an ASIC, etc.) to obtain high speed operation. Using additional gating at the logic circuit **1101**, a processor **1102** may address any of the vector elements in order to use the logic circuit **1101** as a demultiplexer or selector switch.

The element extracted as the "largest" (i.e., a "reference" value) can now be used to normalize the other vector elements. Since the vector elements are log functions (as when amplifiers A1–An are log amplifiers), normalization can be accomplished using digital subtraction circuits DS1–DSn. Specifically, the digital signals from A/D converters A/D1–A/Dn are applied to the positive input of corresponding subtraction circuits DS1–DSn where the "largest" vector element from logic circuit **1101** is subtracted from each. The result will be a negative number for each of the elements (except, of course, for each element equal to the "largest" vector element) that is proportional to the log of the ratio of each element to the reference value.

Next, the processor **1102** polls the element values to rapidly determine which element values are larger than some particular fraction of the energy of the reference value. For example, if the processor is to determine the number of elements whose power is at least 1/e**2 of the reference value, each of the signals output from the digital subtractors DS1–DSn are applied to the positive input of corresponding digital subtraction circuits DSS1–DSSn, and log(1/e**2) **1103** is subtracted therefrom. The elements that have more power than 1/e**2 of the reference value produces a positive value at the output of corresponding subtraction circuits DSS1–DSSn. The elements that have less power produce a negative value at the output of corresponding subtraction circuits DSS1–DSSn.

The signals from the digital subtraction circuits DSS1–DSSn are applied to corresponding sign function (sgn) circuits SGN1–SGNn, each of which output a high or positive signal if the input signal is positive and output a low or negative signal if the input signal is negative. The signals output by the sgn circuits SGN1–SGNn are transmitted to the processor **1102**. A processor (i.e., processor **1102**) having an n bit word can thus identify which of the n element values exceed a particular fraction of the reference power.

With the hardware described above, it is possible to obtain a new vector containing far fewer data bits than the number of bits in the original vector, and yet still have sufficient information to enhance the image processing or other machine vision operation via knowledge of the reflectance properties of the individual pixels.

The diagram of FIG. **12** illustrates an enhancement to the pre-processing circuitry of FIG. **11**. In particular, the logic circuitry illustrated in FIG. **12** replaces logic circuit **1101**. As illustrated, the analog signals from amplifiers A1–An of FIG. **5** are applied to corresponding high speed operational amplifier ("op amp") with diode networks OP1–OPn. The op amp network(s) OP1–OPn corresponding to the largest signal(s) input from amplifiers A1–An generate a positive output signal. The remaining networks OP1–OPn generate a negative output signal.

The signals from networks OP1–OPn are applied to corresponding comparators C1–Cn which convert the positive signals to "1's" and negative signals to "0's." These signals are then each applied to a first terminal of corresponding NAND sample gates N1–Nn.

A negative pulse **1201** resets latches **1202** before each illumination light pulse. This pulse is also inverted by invertor **1203** (after a delay) and applied to each of the second terminals of NAND gates N1–Nn. The signals output by each NAND gate N1–Nn are applied, in parallel, to latches **1202** which latches the applied signals. The signals from latches **1202** are then applied to a selector switch **1204** to select the appropriate signal (i.e., the largest signal) from the signals received from A/D1–A/Dn. The selected signal is then output at output terminal **1205** and may then be used as the reference signal (described above in connection with FIG. **11**).

2-D Bar Code

Determining the reflectance property of each point on a surface is particularly useful in a machine vision application such as reading two-dimensional ("2-D") Bar Codes and data matrix symbols (as described in U.S. Pat. Nos. 4,939,354 and 5,053,609, both expressly incorporated herein by reference). Bar Codes and data matrix symbols are typically generated on a part by altering its local reflectance properties via laser marking, sandblasting, peening, or other means. In the exemplary embodiment, the processor **503** analyzes the information stored regarding each point (e.g., items 1, 5, and

6 above) and generates a two dimensional bit matrix representing the inferred reflectance property of each point illuminated on the object's surface. FIG. **9** illustrates a portion of the generated matrix **910** representing a data matrix symbol sandblasted on a specular surface (such as, for example, stainless steel). Here, a "1" identifies that the corresponding point on the object's surface is highly reflective or specular while a "0" identifies that the point is matte. By analyzing this matrix **910**, the processor can easily decode the two dimensional data matrix symbol.

Surface Orientation

The vector of relative light values gathered for each pixel also provide a means to infer the surface orientation of points or regions illuminated on the object or pattern. As illustrated in FIG. **8**, the normal to the surface at that location may be determined by observing which photodiode detected the highest intensity reflected light, since at approximate locations of the light source **810**, the photodiodes PD1–PD3, and the object **830** are known.

2-D And 3-D Images

As a person of skill in the art will understand, the present invention can be applied to simultaneously obtaining multiple 2-D images of an object, simultaneously obtaining multiple three-dimensional (3-D) images of an object, and simultaneously obtaining both 2-D and 3-D images of an object. One 3-D imaging technique (obtaining a single 3-D image) is described in U.S. Pat. No. 4,957,369 to Antonsson, expressly incorporated herein by reference.

Portable Scanner

It is not necessary to locate the photodetectors and the light source in the same housing, although for certain applications, a common housing may be desirable. A common housing puts all of the optical scanning and photodetection equipment into one easily handled package, and creates a known fixed geometric relationship between the light source and the various photodetectors. This fixed relationship is useful for computing ranges via triangulation and for taking distance and angle into account when determining reflectance properties. The photodetectors may be multi output position sensing devices where a ratio of signals indicates angle and the sum of the signals indicates the light values, as disclosed in U.S. Pat. No. 4,957,369 issued to Antonsson, expressly incorporated herein by reference. However, for portable hand held applications, it may be advantageous to physically separate the functions so that the laser scanning function can be operator held and made as small and lightweight as possible. The photodetectors and processing equipment may be distributed throughout the room or work area where the hand held scanner will be used. Most of the photodetectors, however, should not be shadowed from the area of the object that is being scanned by the light spot.

The object can be located at a large distance from the hand-held laser scanner as long as the laser spot is kept reasonably well focussed on the object surface. There are many ways that focus can be maintained. The simplest are based on normal camera-based autofocus techniques such as sonic ranging, maximizing detail, meter ranging, etc. These known systems can be built into the hand held scanner. Alternatively, the scanner **500** could have its own internal light source (AC or pulsed) used as a target for two photodetectors on a known baseline. This allows the system to track the location of the hand scanner with respect to the known baseline. Since the location of the scanner location and the target location (by tracking a light spot on the object surface), the processor **503** could compute the range between the scanner and the target and use this information to adjust the optics in the scanner to maintain focus.

Other Alternative Embodiments

While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A system for imaging an object comprising:

a light source positioned to transmit light along a first path for illuminating at least a portion of the object;

a first photo sensitive device positioned to detect light reflected from the object at a first preselected position and generating a first signal representing information concerning the light detected;

a photodetector array having a plurality of photodetectors positioned to detect light reflected from the object at a second preselected wherein said photodetector array generates a plurality of second signals representing information concerning the light detected;

a summing amplifier, in communication with the photodetector array, that receives the plurality of second signals and generates a third signal as a function of the plurality of second signals; and

a processor in communication with the first photo sensitive device and the summing amplifier that receives the first signal and generates a first image of the at least a portion of the object as a function of the first signal, and that receives the third signal and generates a second image of the at least a portion of the object as a function of the third signal.

2. The system of claim **1** further comprising:

a lenslet array having a plurality of lenses positioned to focus light reflected from the object onto the photodetector array wherein each lens of the plurality of lenses focusses light onto one of the photodetectors of the plurality of photodetectors.

3. A system for imaging an object comprising:

a light source positioned to transmit light along a first path for illuminating at least a portion of the object;

a first photo sensitive device positioned to detect light reflected from the object at a first preselected position and generating a first signal representing information concerning the light detected;

a photodetector array having a plurality of photodetectors positioned to detect light reflected from the object at a second preselected wherein said photodetector array generates a plurality of second signals representing information concerning the light detected;

a photodetector, in communication with the photodetector array, that receives the plurality of second signals and generates a third signal as a function of the plurality of second signals; and

a processor in communication with the first photo sensitive device and the summing amplifier that receives the first signal and generates a first image of the at least a portion of the object as a function of the first signal, and that receives the third signal and generates a second image of the at least a portion of the object as a function of the third signal.

4. The system of claim **3** further comprising:

a plurality of light guides positioned to transmit the plurality of second signals to the photodetector.

5. A system for imaging a semiconductor package comprising:

a light source positioned to transmit light along a first path for illuminating at least a portion of the semiconductor package;

a first photo sensitive device positioned to detect light reflected from the semiconductor package at a first preselected position and generating a first signal representing information concerning the light detected;

a photodetector array having a plurality of photodetectors positioned to detect light reflected from the semiconductor package at a second preselected wherein said photodetector array generates a plurality of second signals representing information concerning the light detected;

a photodetector, in communication with the photodetector array, that receives the plurality of second signals and generates a third signal as a function of the plurality of second signals; and

a processor in communication with the first photo sensitive device and the summing amplifier that receives the first signal and generates a first image of the at least a portion of the semiconductor package as a function of the first signal, and that receives the third signal and generates a second image of the at least a portion of the semiconductor package as a function of the third signal.

6. The system of claim **5** further comprising:

a plurality of light guides positioned to transmit the plurality of second signals to the photodetector.

* * * * *

US006089763A

United States Patent [19]

Choi et al.

[11] Patent Number: 6,089,763

[45] Date of Patent: Jul. 18, 2000

[54] **SEMICONDUCTOR WAFER PROCESSING SYSTEM**

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[73] Assignee: **DNS Korea Co., Ltd.**, Cheonan, Rep. of Korea

[21] Appl. No.: **09/139,270**

[22] Filed: **Aug. 25, 1998**

[30] **Foreign Application Priority Data**

Sep. 9, 1997	[KR]	Rep. of Korea	97-46236
Sep. 9, 1997	[KR]	Rep. of Korea	97-46237
Sep. 9, 1997	[KR]	Rep. of Korea	97-46238
Sep. 9, 1997	[KR]	Rep. of Korea	97-46239
Sep. 9, 1997	[KR]	Rep. of Korea	97-46240
Sep. 9, 1997	[KR]	Rep. of Korea	97-46241
Sep. 9, 1997	[KR]	Rep. of Korea	97-46242
May 12, 1998	[KR]	Rep. of Korea	98-16904

[51] **Int. Cl.**[7] **G03D 5/00**; H01L 21/00

[52] **U.S. Cl.** **396/611**; 396/570; 396/627; 414/225; 414/935

[58] **Field of Search** 396/604, 611, 396/624, 627, 630, 570, 578; 414/152, 225, 935, 941; 430/30; 355/27, 53

[56] **References Cited**

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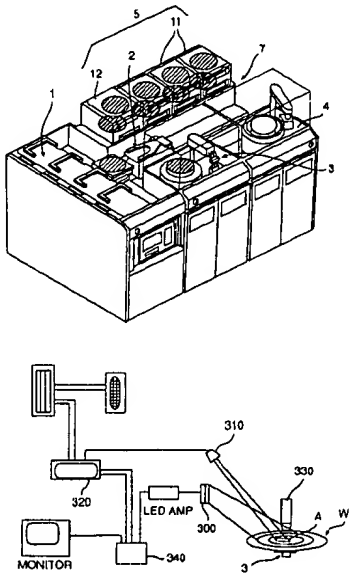
Primary Examiner—Alan A. Mathews

[57] **ABSTRACT**

A semiconductor wafer processing system having a multi-layered arrangement of wafer processing units included in a spinner to carry out photoresist coating and developing processes for the formation of micro patterns on semiconductor wafers, thereby enabling an easy increase in those processing units coping with an introduction of new processes without increasing the occupying space of the processing units, while being capable of achieving accurate wafer feeding and loading operations, and minimizing the consumption of a chemical solvent coated over wafers. The system includes groups of modules each being selected from first and second modules. The first module includes a plurality of bake units each having bake boxes arranged in a multi-layered fashion, the bake units being arranged adjacent to one another in the wafer feeding direction, and a spin unit, such as a spine coater or a spine developer, fixedly mounted on the bake units. The second module includes a plurality of wafer edge exposure units arranged in a multi-layered fashion while being arranged in such a fashion that they are adjacent to one another in the wafer feeding direction, and a spin unit fixedly mounted on the wafer edge exposure units. Each module group constitute a station, together with a feeding robot. A feeing interface or buffer stocker is arranged between adjacent stations.

16 Claims, 13 Drawing Sheets



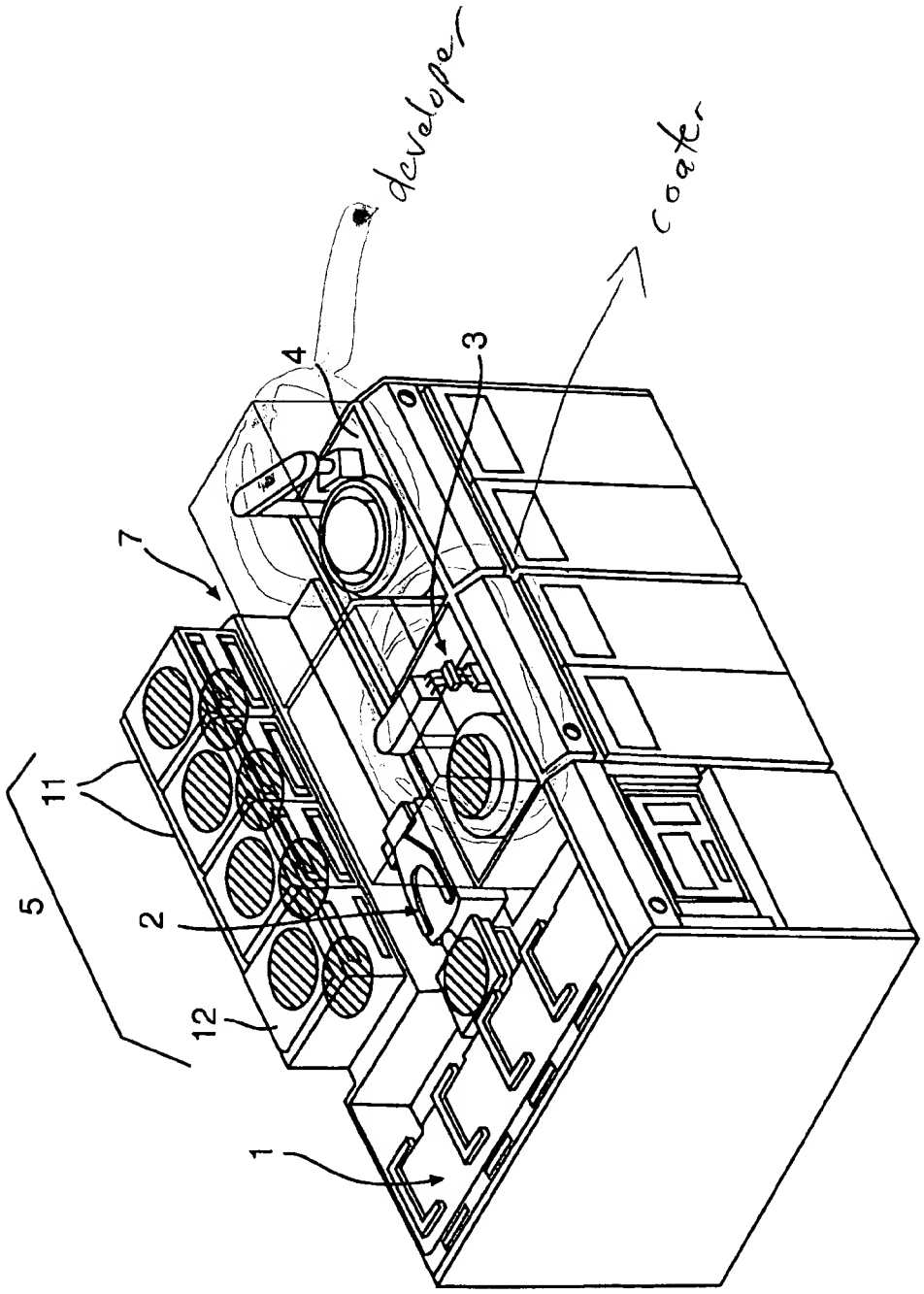
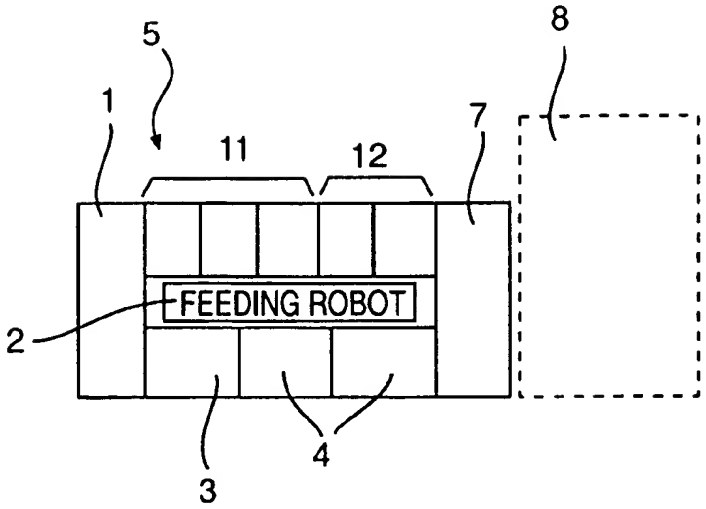


FIG. 1a


5
8
1
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12
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FEEDING ROBOT
2
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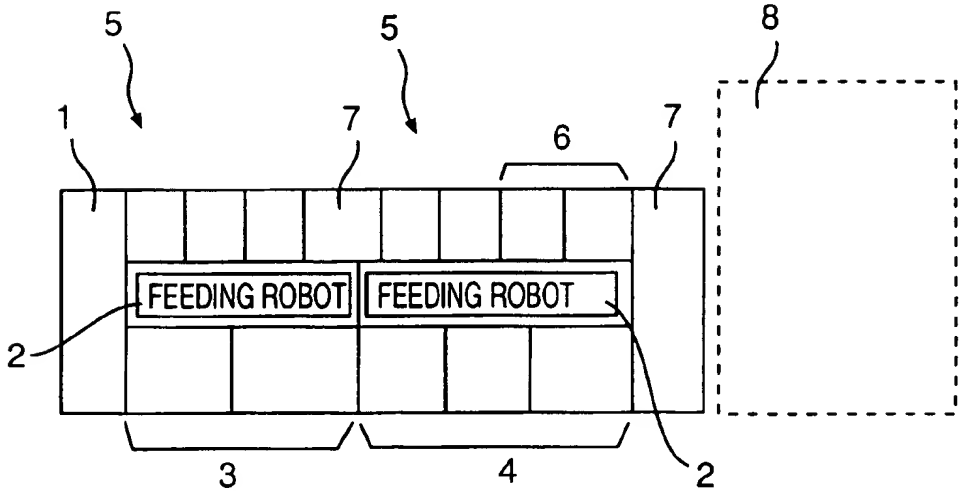
FIG. 1b


5
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FEEDING ROBOT
FEEDING ROBOT
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2

FIG. 1c

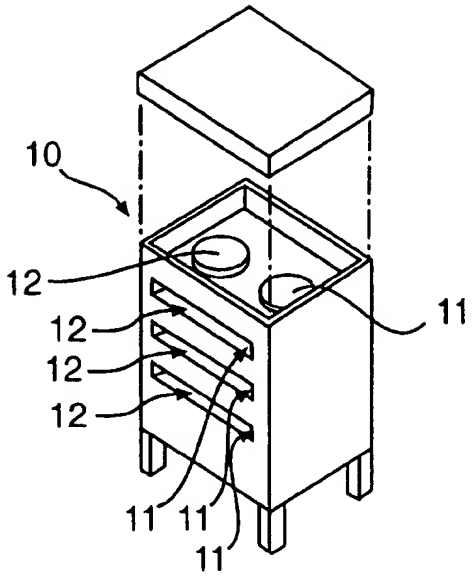

FIG. 2

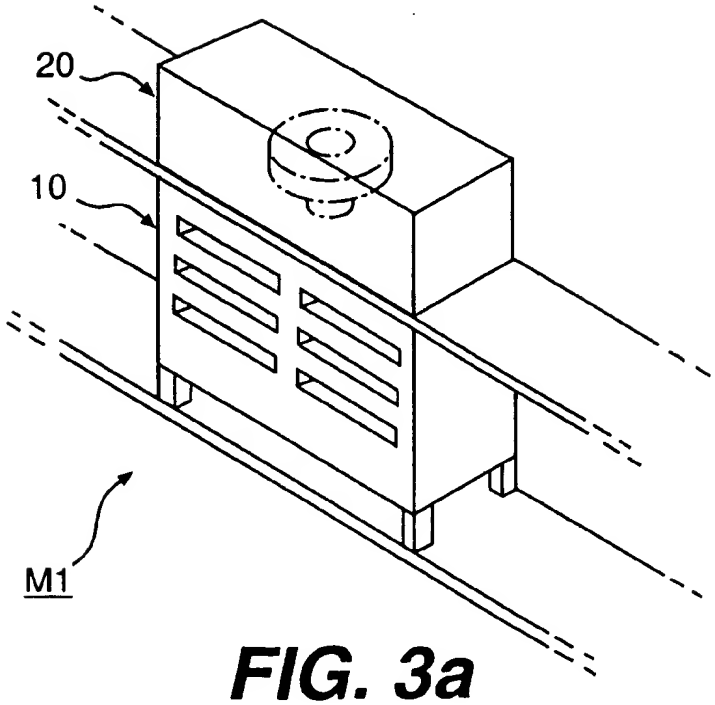

FIG. 3a

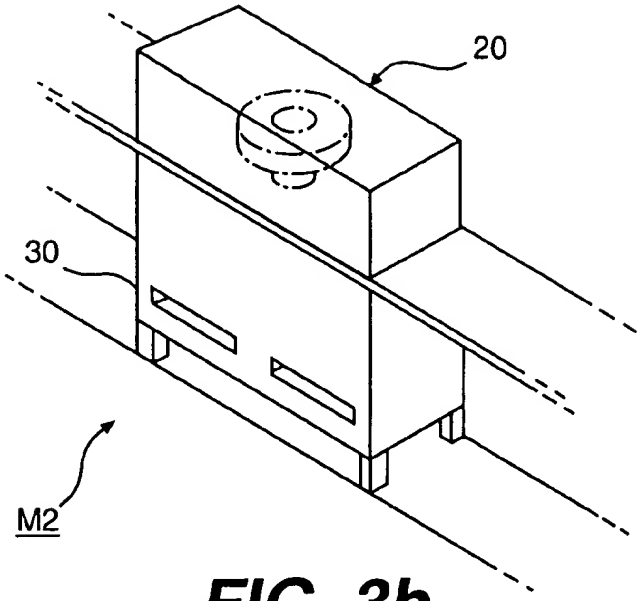

FIG. 3b

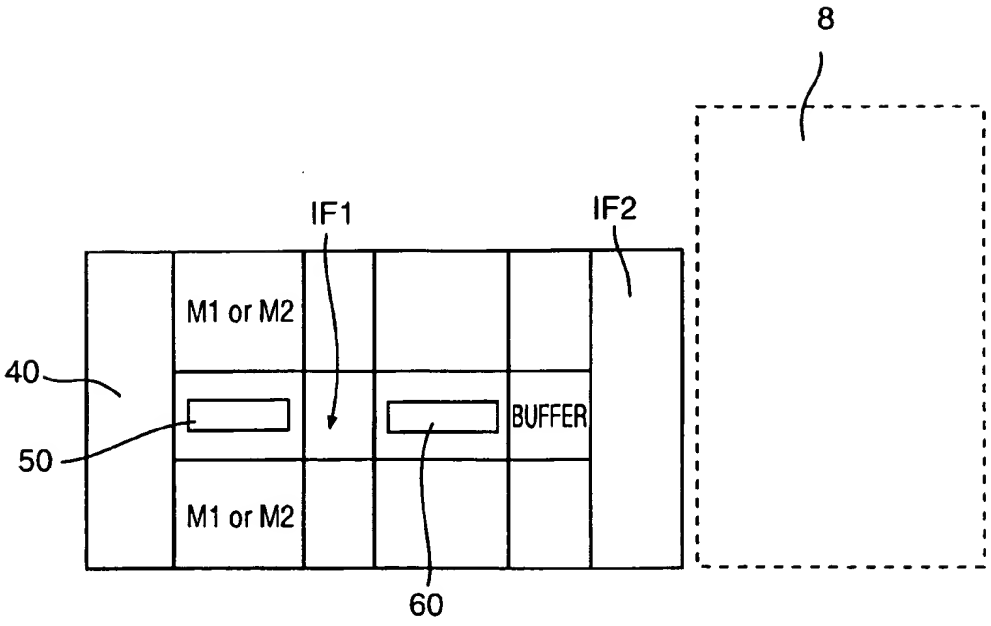

FIG. 4

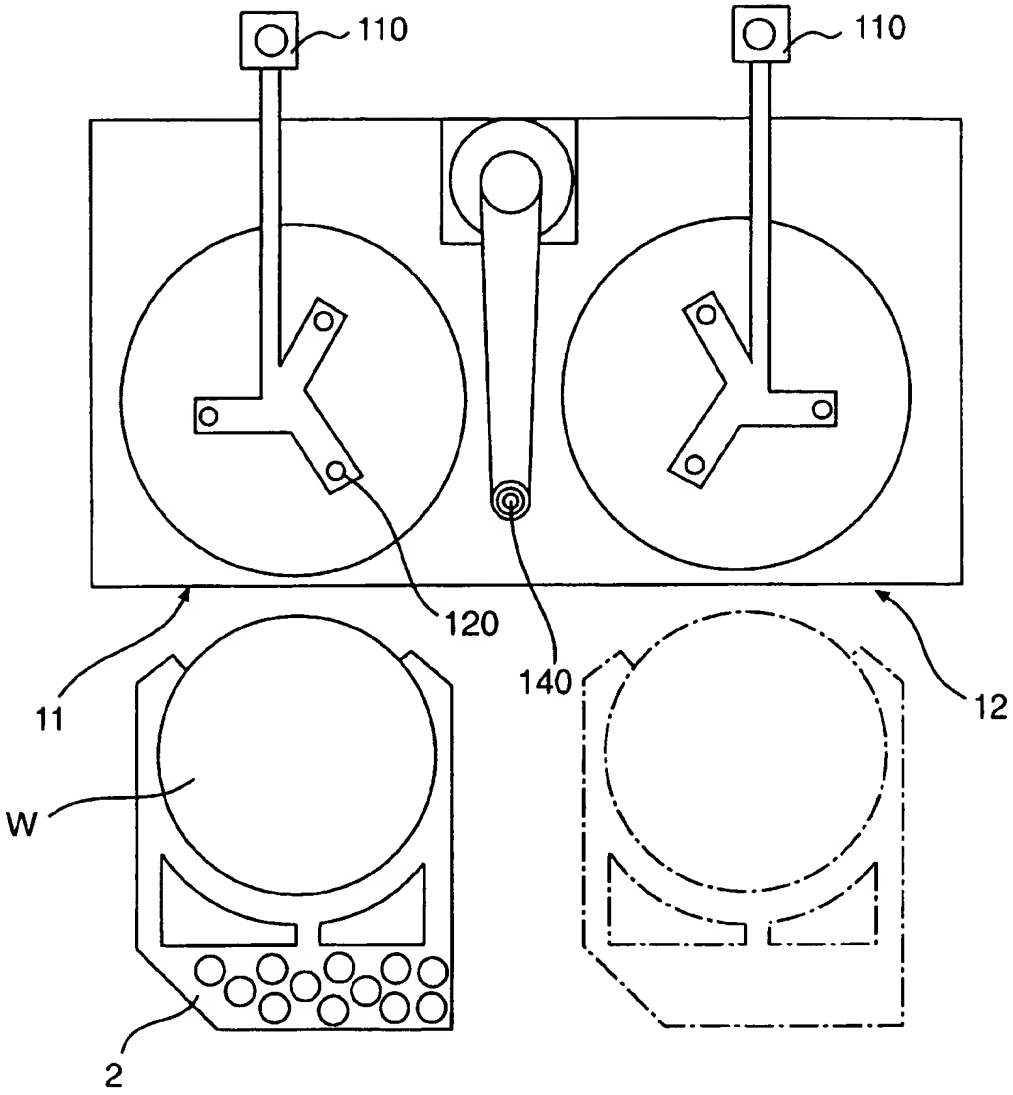

FIG. 5a

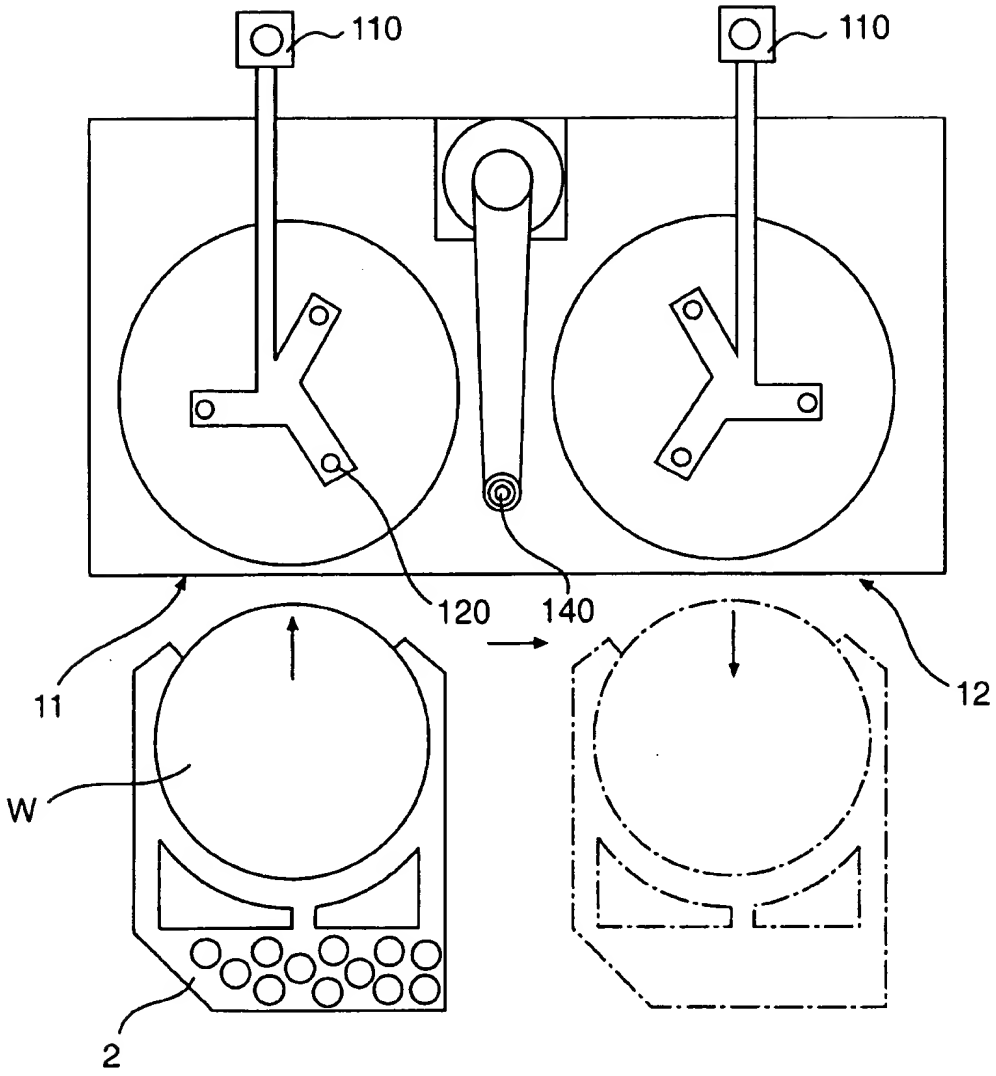

FIG. 5b

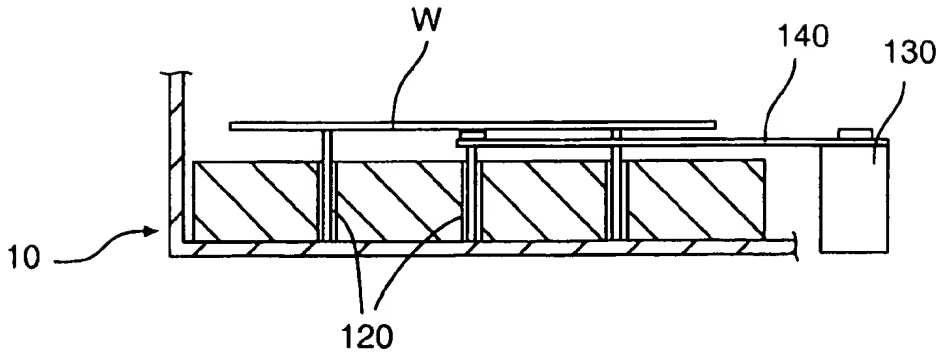

FIG. 5c

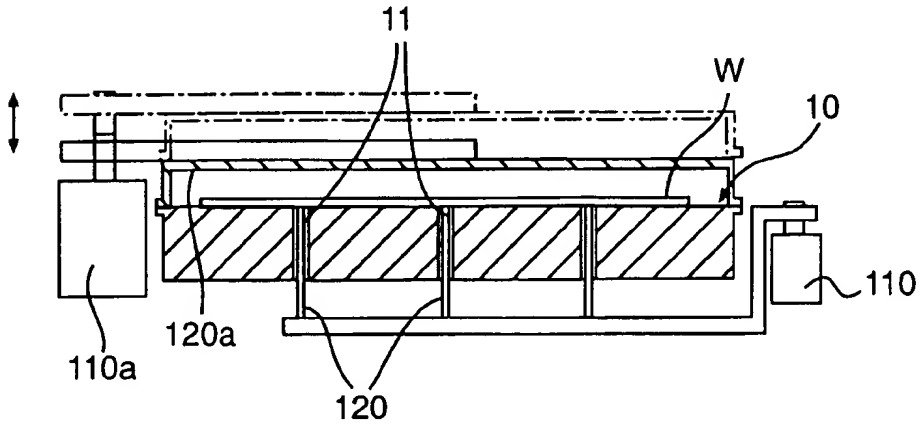

FIG. 7

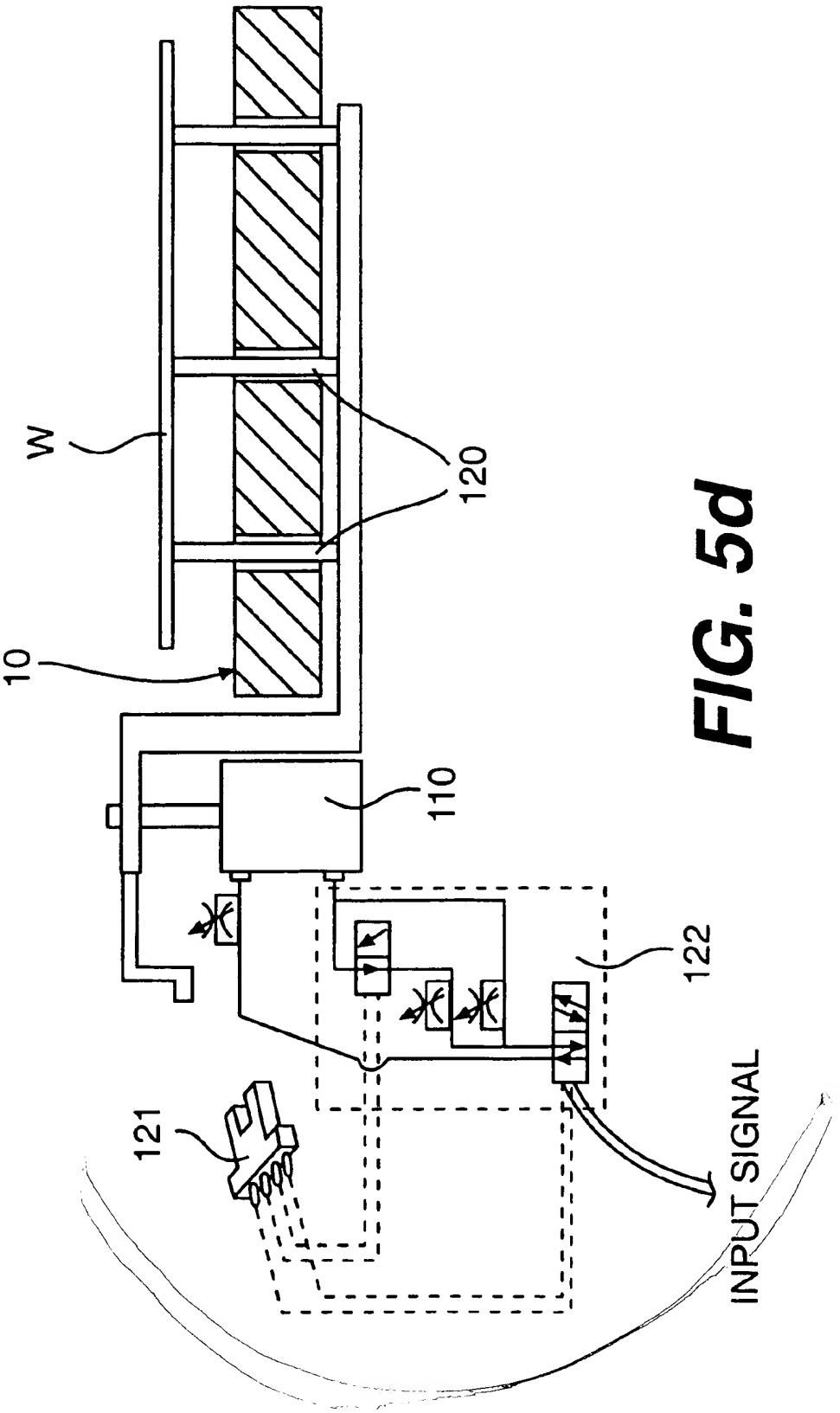

FIG. 5d

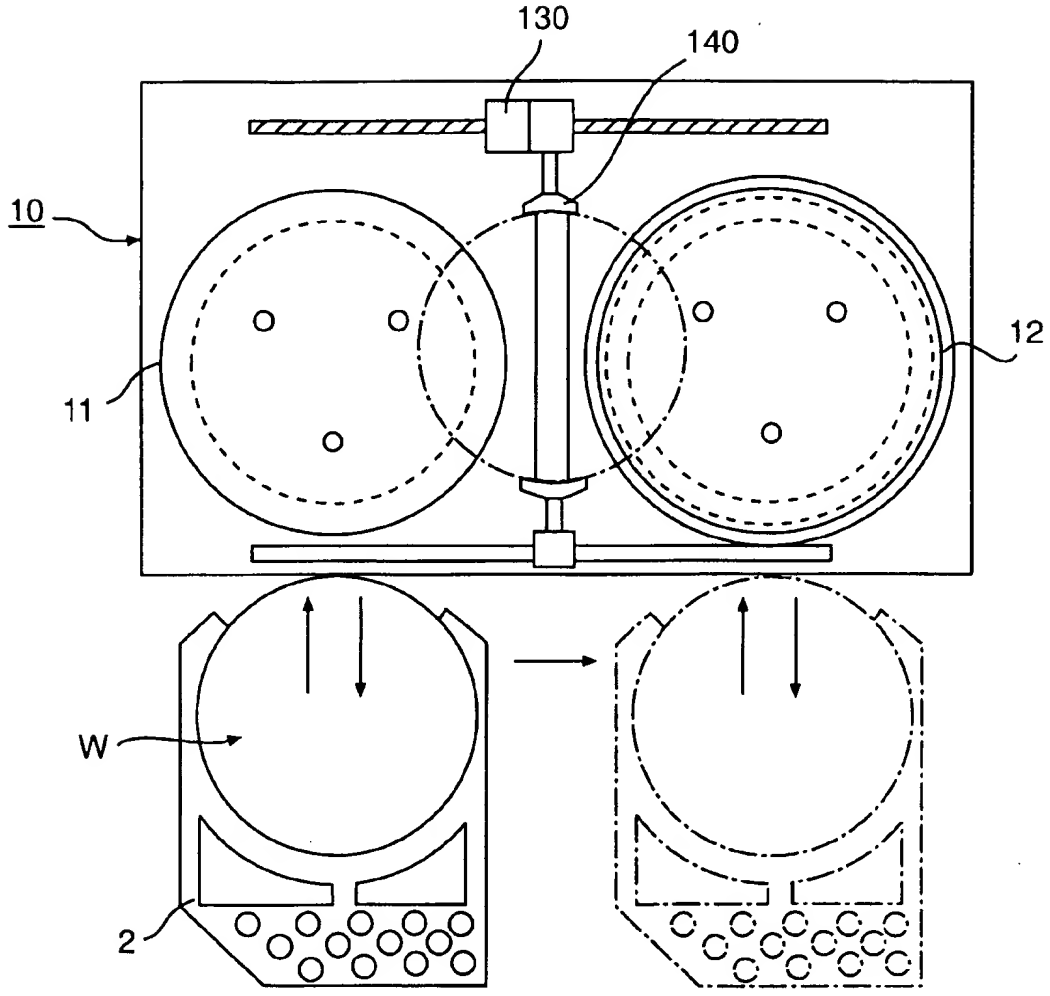

FIG. 6

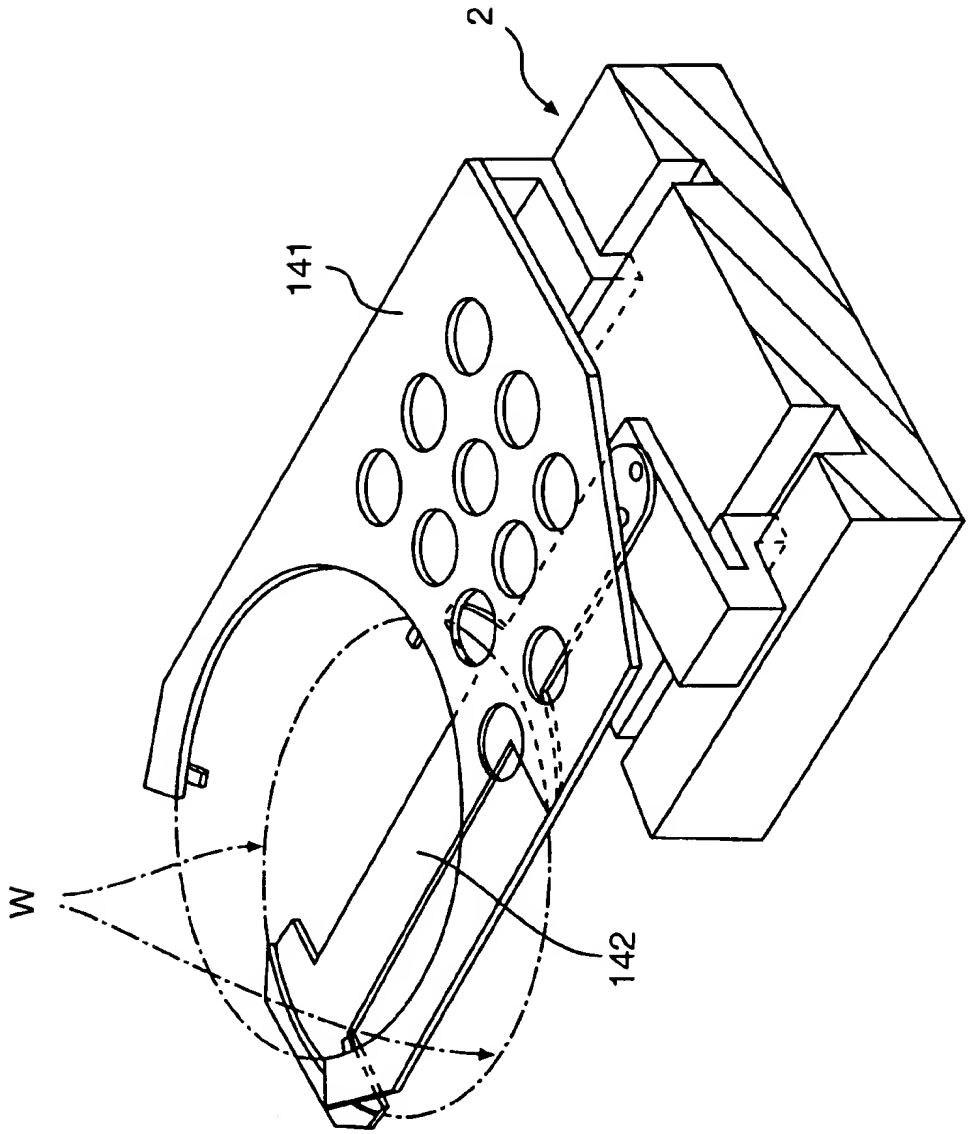

FIG. 8

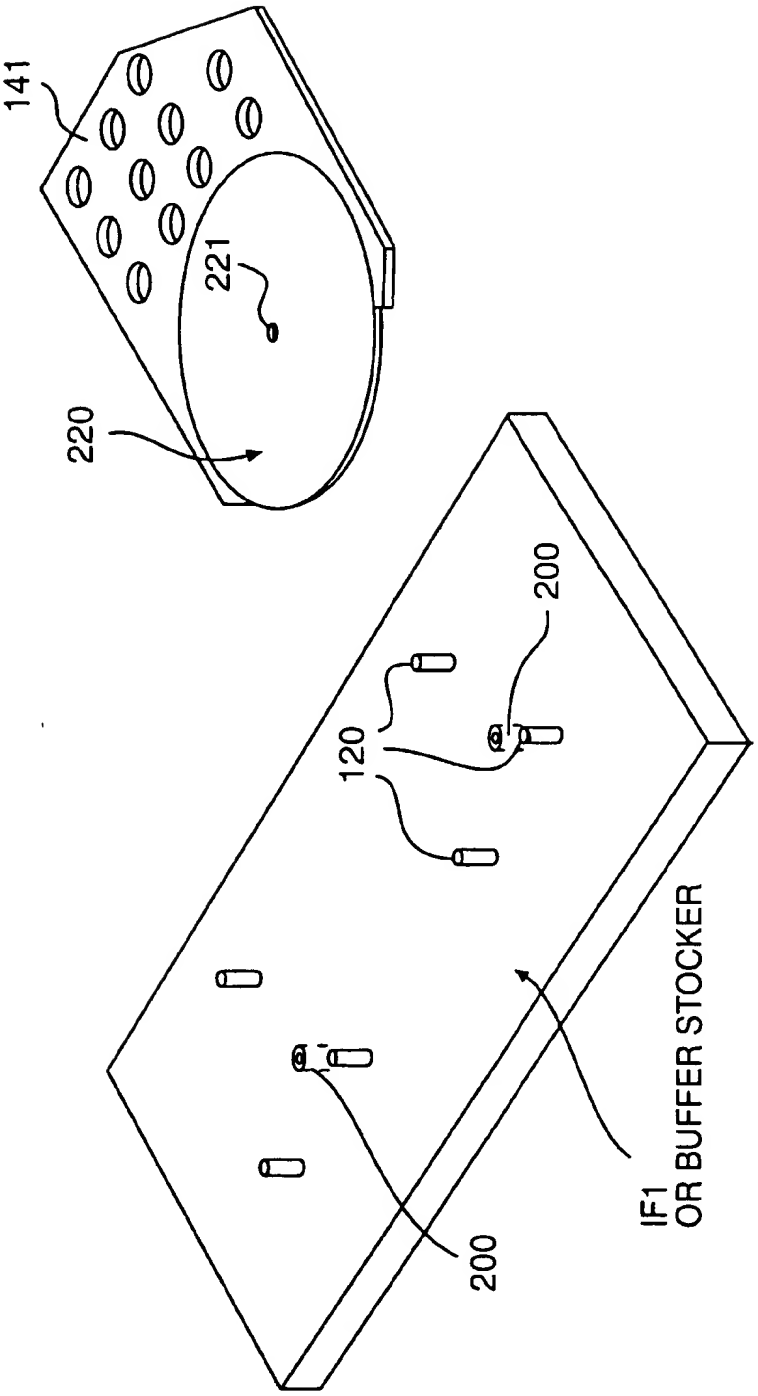

FIG. 9

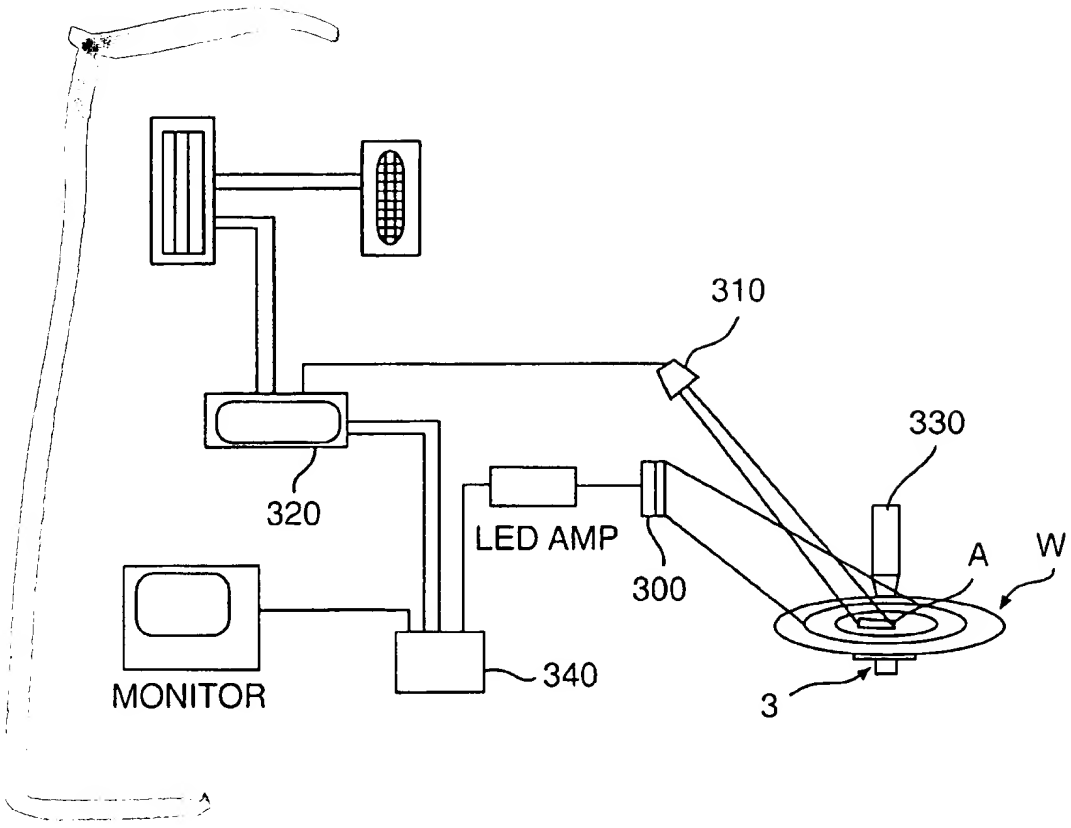

FIG. 10

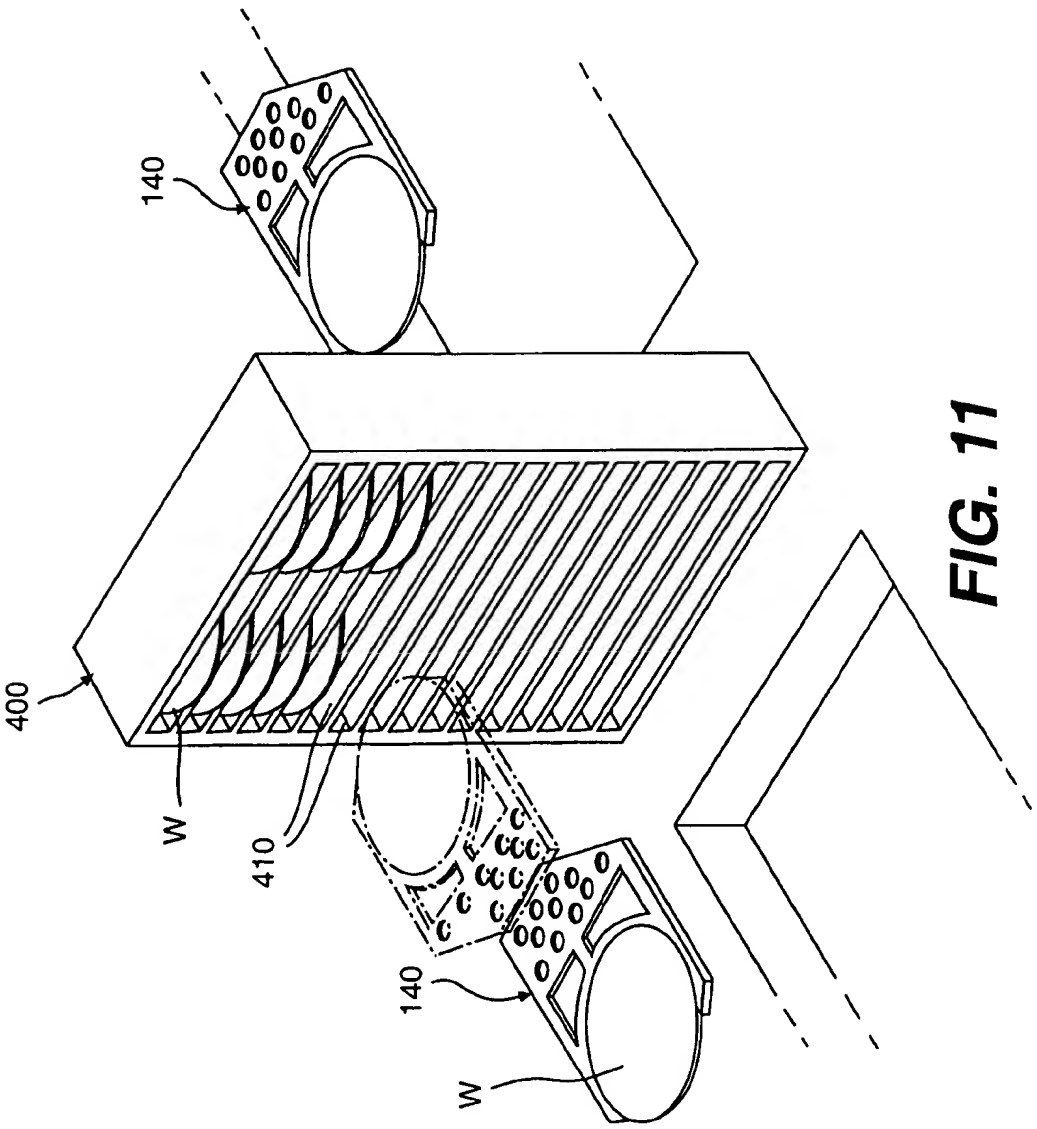

FIG. 11

SEMICONDUCTOR WAFER PROCESSING SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a system for processing semiconductor wafers, and more particularly to a semiconductor wafer processing system having a multi-layered arrangement of wafer processing units included in a spinner to carry out photoresist coating and developing processes for the formation of micro patterns on semiconductor wafers, thereby enabling an easy increase in those processing units coping with an introduction of new processes without increasing the occupying space of the processing units, while having a configuration capable of achieving accurate wafer feeding and loading operations, and minimizing the consumption of a chemical solvent coated over wafers.

2. Description of the Prior Art

As well known, a photo-lithography process is an important process in the processing of semiconductor wafers. Such a photo-lithography process is carried out using an integrated coating and developing installation which performs a coating process for coating a photoresist solution over a wafer, a baking process for the coated photoresist, and a developing process for the baked photoresist. The integrated coating and developing installation is connected with a stepper in an in-line manner via an interface. Such an integrated coating and developing installation is an important device for the formation of micro patterns on wafers, namely, the fabrication of highly integrated semiconductor devices.

Meanwhile, a variety of new techniques requiring an introduction of new processes have also been proposed for the fabrication of semiconductor devices with a super integration degree. Furthermore, the recent trend to use wafers with an increased size has resulted in an increase in the scale of wafer processing installations and a complexity in the arrangement of wafer processing installations.

FIGS. **1***a* and **1***b* are a perspective view and a plan view respectively illustrating a general spinner. As shown in FIGS. **1***a* and **1***b*, the spinner includes an indexer **1** for carrying out wafer loading and unloading operations, a feeding robot **2** for feeding a loaded wafer to processing units, respectively, a spin coater **3** for coating a photoresist solution over the wafer, and a spin developer **4** for developing the wafer subjected to a light exposure. A bake unit **5** is also provided which includes a hot plate **11** and a cool plate **12** respectively adapted to heat and cool the wafer before or after the photoresist coating or developing process. The spinner further includes a wide expose edge (WEE) unit **6** for exposing to light an unnecessary portion of the photoresist disposed on the peripheral edge portion of the wafer, and an interface **7** provided with a stocker interacting with an additional stepper **8** arranged adjacent to the WEE unit **6**.

Although such a conventional installation may have a variable combination of processing units in accordance with processes to be carried out, it requires a relatively large installation area occupying a large portion of the entire semiconductor fabrication line because most processing units thereof are arranged in a planar manner, as shown in FIG. **1***b* or **1***c*.

For this reason, additions of processing units and new installations, involved due to an introduction of new processes and use of wafers increased in diameter, result in

requirement of an increased installation area. This results in an increase in the area to be managed. Such an increase in the area to be managed results in an increase in manufacturing costs because the semiconductor fabrication line should essentially be in a super-clean environment. Furthermore, the entire fabrication line should be modified in design due to the introduction of new processes and the use of additional processing units or increased installation area caused by the use of enlarged wafers.

In order to solve such problems, a variety of techniques have been proposed. For example, a technique has been proposed in which a single feeding means is used to feed a workpiece (namely, a wafer) from a designated area to processing chambers. In accordance with this technique, a plurality of processing chambers are arranged in a multi-layered fashion around the feeding means in order to reduce the entire installation area.

Where this technique is applied to the fabrication of highly integrated semiconductor products of a 64 Mega grade or higher, requiring increased numbers of spin coaters, spin developers and bake units, it is inevitably necessary for those processing units to be arranged on three layers or more in order to achieve desired processes in each processing station using the single feeding means.

In the case of compact processing units such as bake units, a relatively easy multi-layered arrangement is achieved. However, where bulky processing units such as spin coaters or spin developers, which are important units for the processing of wafers, are arranged in a multi-layered fashion on three floors or more, the installation has a height of 3.5 m or more. For this reason, there is a great difficulty in the manufacture, repair, and maintenance of the installation. Furthermore, abnormal spaces are required on the semiconductor fabrication line which requires a super-clean state. For this reason, there is a problem in that the entire semiconductor fabrication line should be modified or newly designed.

Moreover, the single feeding means may be overloaded in the process of loading wafers into a plurality of processing chambers (at least 15 processing chambers) arranged in a multi-layered fashion around the feeding means or unloading wafers from those processing chambers. In this case, a degradation in the efficiency of the installation and a degradation in productivity may occur. In addition, there is a limitation in the space for occupying a variety of processing units required for the fabrication of semiconductor products with a super integration degree. Such a limited occupying space results in a great limitation in the use of processing units respectively required for achieving a variety of processes.

SUMMARY OF THE INVENTION

The present invention has been made in view of the above mentioned problems involved in conventional integrated coating and developing installations for semiconductor wafers, and an object of the invention is to provide a semiconductor wafer processing system capable of minimizing the area for occupying processing units even when an addition of processing units is required due to an introduction of new processes and use of wafers increased in diameter.

Another object of the invention is to provide a semiconductor wafer processing system including a plurality of robot arms selectively operating to accurately feed a wafer and to accurately load the fed wafer on a desired position, thereby being capable of preventing a degradation in the quality of products due to a feeding delay and an inaccurate loading.

Another object of the invention is to provide a semiconductor wafer processing system capable of controlling the amount of a solvent supplied upon coating a photoresist solution over a wafer while controlling the rotating speed of the wafer, thereby achieving an improvement in the stability and reliability of the coating process and a minimized consumption of the solvent.

In accordance with the present invention, these objects are accomplished by providing a semiconductor wafer processing system comprising groups of modules each being selected from first and second modules. The first module includes a plurality of bake units each having a plurality of bake boxes arranged in a multi-layered fashion, the bake units being arranged in such a fashion that they are adjacent to one another in the wafer feeding direction, and a spin unit, such as a spine coater or a spine developer, fixedly mounted on the bake units. The second module includes a plurality of wafer edge exposure units arranged in a multi-layered fashion while being arranged in such a fashion that they are adjacent to one another in the wafer feeding direction, and a spin unit, such as a spine coater or a spine developer, fixedly mounted on the wafer edge exposure units. Each module group constitutes a station, together with a feeding robot. A feeding interface or buffer stocker is arranged between adjacent stations.

Accordingly it is possible to minimize the area for occupying processing units even when an addition of processing units is required due to an introduction of new processes and use of wafers increased in diameter. It is also possible to accurately feed a wafer and to accurately load the fed wafer on a desired position. The semiconductor wafer processing system can also efficiently carry out a photoresist coating operation, thereby achieving an improvement in productivity.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and aspects of the invention will become apparent from the following description of embodiments with reference to the accompanying drawings in which:

FIGS. **1***a* and **1***b* are a perspective view and a plan view respectively illustrating a general spinner;

FIG. 1*c* is a plan view illustrating another spinner;

FIG. **2** is a perspective view schematically illustrating a bake unit applicable to the spinners in accordance with an embodiment of the present invention;

FIGS. **3***a* and **3***b* are perspective views respectively illustrating a module configured by bake units and a spin coater or spin developer and a module configured by WEE units and a spin coater or spin developer;

FIG. **4** is a plan view illustrating a semiconductor wafer processing system in which the modules of FIGS. **3***a* and **3***b* are incorporated in accordance with the present invention;

FIG. **5***a* is a plan view illustrating a feeding arm adapted to feed a wafer to each bake unit in accordance with the present invention;

FIGS. **5***b* and **5***c* are a plan view and a cross-sectional view respectively illustrating an operation of the feeding arm shown in FIG. **5***a;*

FIG. **5***d* is a view schematically illustrating means for controlling wafer supporting pins adapted to load a wafer on each plate of a bake unit;

FIG. **6** is a plan view illustrating another embodiment of the feeding arm shown in FIG. **5***a;*

FIG. **7** is a sectional view illustrating the opened and closed states of each plate of the bake unit achieved by a cover member;

FIG. **8** is a perspective view illustrating a detailed configuration of a feeding robot provided with wafer feeding arms;

FIG. **9** is a perspective view illustrating means for setting a wafer loading position of each wafer feeding arm in accordance with the present invention;

FIG. **10** is a block diagram illustrating an apparatus for controlling the supply of a coating solvent upon coating a photoresist solution over the surface of a wafer in accordance with the present invention; and

FIG. **11** is a perspective view illustrating a stocker arranged between the spinner and a stepper in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. **1***a,* an example of a spinner, namely, an integrated installation for coating a photoresist solution over a semiconductor wafer, and developing the coated photoresist, is illustrated to which the present invention is applied. As described above in conjunction with FIG. **1***a,* the spinner includes an indexer **1** for carrying out wafer loading and unloading operations, a feeding robot **2** for feeding a loaded wafer to processing units, respectively, a spin coater **3** for coating a photoresist solution over the wafer, and a spin developer **4** for developing the wafer subjected to a light exposure, a bake unit **5** provided with hot plates **11** and cool plates **12** respectively adapted to heat and cool the wafer before or after the photoresist coating or developing process, a WEE unit **6** for exposing to light an unnecessary portion of the photoresist disposed on the peripheral edge portion of the wafer, and an interface **7** provided with a stocker interacting with an additional stepper **8** arranged adjacent to the WEE unit **6**.

FIG. **2** schematically illustrates a bake unit applicable to the above mentioned spinner in accordance with an embodiment of the present invention. As shown in FIG. **2**, the bake unit, which is denoted by the reference numeral **10**, includes a plurality of bake boxes arranged in a multi-layered fashion. In each bake box, a pair of plates are arranged side by side with each other. The plates arranged in each bake box may include a hot plate **11** adapted to heat a wafer fed to the bake box and a cool plate **12** adapted to cool the wafer, as shown in FIG. **2**. Alternatively, both plates arranged in each bake box may include hot plates **11** or cool plates **12**.

Taking the management of the bake unit **10** into consideration, it is preferred that the number of multi-layered bake boxes in the bake unit **10** be ten or less. Since the bake unit **10** consists of bake boxes arranged in a multi-layered fashion, the area occupied by the bake unit **10** can be minimized. Furthermore, there is no increase in the area occupied by the bake unit **10** when the hot and cool plates **11** and **12** of the bake unit **10** should increase in number to increase the capacity of the bake unit **10**. This is because the increase in the capacity of the bake unit **10** can be accomplished by simply layering, in the bake unit **10**, additional bake boxes containing the increased number of hot and cool plates **11** and **12**. Even when two or more bake units **10** should be used, it is possible to minimize an increase in the area occupied by those bake units **10** by virtue of the above mentioned multi-layered arrangement.

FIG. **3***a* illustrates a module consisting of a plurality of bake units and a spin coater or spin developer laid on the bake units. The module of FIG. **3***a,* namely, a first module **M1**, includes two bake units **10** arranged adjacent to each other, and a spin unit **20** fixedly mounted on the bake units

10. The spin unit 20 consists of a spin coater or spin developer. If necessary, the first module M1 may have an increased number of bake units 10. Each bake unit 10 includes a plurality of bake boxes arranged in a multi-layered fashion.

Since the first module M1 consists of a plurality of bake units 10 arranged adjacent to one another, each bake unit 10 consisting of multi-layered bake boxes, and the spin unit 20 laid on the bake units 10, it is possible to minimize an increase in installation area caused by the provision of additional processing units, namely, additional bake units 10. By such an arrangement, it is also possible to minimize the movement range of the feeding robot moving among processing units. This results in a reduction in operating time and an improvement in performance.

FIG. 3*b* illustrates a module consisting of a plurality of WEE units and a spin coater or spin developer laid on the units. The module of FIG. 3*b*, namely, a second module M2, includes two WEE units 30 arranged adjacent to each other, and a spin unit 20 fixedly mounted on the WEE units 30. The spin unit 20 consists of a spin coater or spin developer. If necessary, the second module M2 may have an increased number of WEE units 30 arranged in a multi-layered fashion.

Since the second module M2 consists of a plurality of WEE units 30, which may be arranged adjacent to one another while also being arranged in a multi-layered fashion, it is possible to minimize an increase in installation area caused by the provision of additional processing units, namely, additional WEE units 30. By such an arrangement, it is also possible to achieve a reduction in operating time and an improvement in performance.

FIG. 4 is a plan view illustrating a semiconductor wafer processing system in which the above mentioned modular units are incorporated in accordance with the present invention. As shown in FIG. 4, a first robot 50 is arranged downstream from an indexer 40 adapted to carry out wafer loading and unloading operations. The first robot 50 serves to feed a wafer loaded by the indexer 40 to a desired processing unit. Modules are arranged in opposite sides of the first robot 50, respectively. The modules may include first and second modules M1 and M2 respectively having the above mentioned configurations. Alternatively, the modules may be first modules M1 or second modules M2.

A second robot 60 is arranged downstream from the first robot 50 in such a fashion that it is aligned with the first robot 50. A first interface IF1 is arranged between the first and second robots 50 and 60. Modules are arranged in opposite sides of the second robot 60, respectively. The modules may include first and second modules M1 and M2 respectively having the above mentioned configurations. Alternatively, the modules may be first modules M1 or second modules M2. Downstream from the second robot 60, a stepper 70 is arranged which serves to expose the entire portion of a wafer coated with photoresist. A buffer stocker and a second interface IF2 are arranged between the second robot 60 and the stepper 70.

In accordance with the present invention, the semiconductor wafer processing system includes at least two wafer processing stations having the above mentioned basic arrangement. That is, each wafer processing station includes a feeding means, and modules arranged in opposite sides of the feeding means. Each wafer processing station may include at least two modules arranged in a multi-layered fashion in each side of the feeding means. The modules arranged in each side of the feeding means may include first and second modules M1 and M2 respectively having the above mentioned configurations. Alternatively, the modules may be first modules M1 or second modules M2. A feeding interface or buffer stocker is arranged between adjacent stations. By such an arrangement, the occupying area of the entire installation can be minimized. In addition, it is possible to efficiently achieve the entire process.

FIG. 5*a* illustrates a feeding arm adapted to feed a wafer to each bake unit in accordance with the present invention. FIGS. 5*b* and 5*c* are a plan view and a cross-sectional view respectively illustrating an operation of the feeding arm shown in FIG. 5*a*. Referring to FIG. 5*a*, a bake unit 10 is illustrated which includes a pair of plates, namely, the hot and cool plates 11 and 12. For each of the hot and cool plates 11 and 12, a plurality of support pins 120 are arranged in such a fashion that they move vertically through vertical holes provided at the plate to vertically move a wafer between a position, in which the wafer is loaded on the plate, and a position, in which the wafer is unloaded from the plate. The vertical movement of the support pins 120 for each plate is achieved by a reciprocal operation of a cylinder 110 connected to the support pins 120. The feeding robot 2, which serves to carry out loading and unloading operations for wafers, is arranged in the vicinity of the bake units 10.

The feeding arm, which is denoted by the reference numeral 140, is arranged in a space defined between the hot and cool plates 11 and 12. The feeding arm 140 is independently driven by a separate drive means 130 so that it moves pivotally between the hot and cool plates 11 and 12. A wafer holding member is provided at a free end of the feeding arm 140.

Preferably, the wafer holding member has a configuration capable of holding a wafer by sucking the central portion of the lower surface of the wafer using vacuum pressure. Alternatively, the wafer holding member may have a configuration capable of gripping the peripheral portion of the wafer at opposite sides of the wafer. The feeding arm 140 moves between the hot and cool plates 11 and 12 to feed a wafer under the condition in which the wafer is held by the wafer holding member.

In the illustrated case, a wafer, which is denoted by the reference character W, is first fed by the feeding arm 140 to the hot plate 11 which serves to heat the wafer W at a set temperature for a set time. Just after the heating process is completed, the wafer W is fed to the cool plate 12 by the feeding arm 140 so that it is subjected to a subsequent cooling process. The feeding of the wafer W is carried out irrespective of the operation of the feeding robot 2. Accordingly, it is possible to allow the wafer W to wait safely for a subsequent process in a state laid on the cool plate 12.

As shown in FIG. 5*d*, the support pins 120, which extend vertically through the hot and cool plates 11 and 12, thereby supporting the wafer W in a horizontal state in accordance with a vertical movement of the cylinder 110, is controlled by a controller 122. A position sensor 121, which serves to sense a moved position of the support pins 120, is electrically coupled to the controller 122. The controller 122 generates a control signal for controlling the support pins 120, based on a signal from the position sensor 121 indicative of the moved position of the support pins 120. Preferably, the controller 122 controls the vertical movement of the support pins 120 in such a fashion that the support pins 120 supporting the wafer W move at a high speed at the initial stage of their downward movement for loading the wafer W on the hot or cool plate while moving

at a low speed at a stage of the downward movement just before the wafer W comes into contact with the plate. The support pins **120** are also controlled to move at a high speed when they are separated from the wafer W. In accordance with such a controlled movement of the support pins **120**, it is possible to prevent the wafer from being horizontally slipped or shifted due to air resistance when it is seated on the hot or cool plate, thereby accurately loading the wafer on a desired position.

FIG. **6** illustrates another embodiment of the feeding arm. Referring to FIG. **6**, a feeding arm **140** is illustrated which slides between the hot and cool plates **11** and **12** by the drive means **130** along guides respectively arranged in opposite sides of the hot and cool plates **11** and **12**. Only one guide may be provided which is arranged in one side of the hot and cool plates **11** and **12**.

The wafer W, which has been completely subjected to heating and cooling processes on the hot and cool plates **11** and **12** of the bake unit **10**, waits a desired time in the interior of the bake unit **10** until a subsequent wafer is fed to the bake unit **10**. During the waiting of the wafer W, the inner temperature of the bake unit **10** is transferred to the wafer W. Such a thermal transfer influences the yield of final products. Therefore, it is important to maintain the wafer W at a desired temperature during its waiting state, in terms of the quality.

To this end, cover members **120***a* are provided for the hot and cool plates in accordance with the present invention, as shown in FIG. **7**, so as to prevent ambient air from being introduced into the interior of the bake unit **10** during the waiting period of the wafer W. Each cover member **120***a* is arranged above the hot or cool plate to move vertically with respect to the plate in accordance with an operation of a separate cylinder **110***a*, thereby opening and closing the plate. The cylinder **110***a* operates independently of the cylinder **110** adapted to drive the support pins **120**.

Each cover member **120***a* is maintained at a position, where it opens the associated plate, when the wafer loading or unloading operation is carried out. During the waiting period of the wafer W, the cover member **120***a* is maintained at a position where it closes the associated plate. Thus, the cover member **120***a* maintains the associated wafer in a heated or cooled state without causing any variation in the heated or cooled temperature of the wafer. Accordingly, it is possible to achieve an improvement in the yield of final products.

FIG. **8** is a perspective view illustrating a detailed configuration of the feeding robot **2** which is provided with wafer feeding arms. As shown in FIG. **8**, the feeding robot **2**, which moves to feed a wafer to a set position for each unit of the spinner, thereby loading the wafer to the set position or unloading the wafer from the set position, includes a pair of wafer feeding arms **141** and **142** each adapted to feed a wafer while holding the wafer. The wafer feeding arm **141** has a plate shape and serves to support the peripheral portion of a wafer whereas the wafer feeding arm **142** has a bar shape and serves to support the portion of the wafer extending diametrically through the center of the wafer. In accordance with the characteristics of a processing unit, in which a wafer is loaded, a selected one of the wafer feeding arms **141** and **142** operates to feed the wafer.

By such a configuration, it is unnecessary to replace the wafer feeding arms of the feeding robot with new ones in accordance with the characteristics of support means or processing units. This is possible by virtue of the use of a selected one of the wafer feeding arms. Accordingly, it is possible to enhance the wafer feeding efficiency.

Meanwhile, it is important to accurately load a wafer W on a desired position when the wafer W is loaded on the first interface or buffer stocker using the feeding robot provided with the wafer feeding arms **141** and **142**. In particular, the first interface and buffer stocker are arranged at positions preventing the user from directly observing those units with the naked eye. To this end, a reflex sensor **200** is provided, as a means for accurately setting a desired wafer loading position, in accordance with the present invention. As shown in FIG. **9**, the reflex sensor **200** is arranged on the plate of each processing unit, which is a bake unit **10** in the case illustrated in FIG. **9**, at a position corresponding to the center of a wafer accurately loaded on the plate. In other words, the reflex sensor **200** is arranged in such a fashion that it radiates a light beam onto the center of the lower surface of the accurately loaded wafer. A jig wafer **220** is also used to accurately determine a desired wafer loading position. A through hole **221** is formed through the central portion of the jig wafer **220** so that the light beam emitted from the reflex sensor **200** passes through the through hole **221** when the jig wafer **220** is accurately loaded at a desired wafer loading position on the plate by the feeding robot. Accordingly, the wafer loading position of the feeding robot can be accurately set to correspond to a desired wafer loading position by determining whether the light beam emitted from the reflex sensor **200** transmits through the jig wafer **220** loaded by the feeding robot or reflects from the jig wafer **220**.

That is, the jig wafer **220** is first loaded on the plate by the wafer feeding arm **141** or **142** of the feeding robot, at the initial stage of the wafer loading operation. In this state, it is determined whether or not the light beam emitted from the reflex sensor **200** transmits through the jig wafer **220** or reflects from the jig wafer **220**. Based on a signal from the reflex sensor **200** indicative of the result of the above determination, the wafer loading position of the feeding robot is adjusted so that it corresponds to a desired wafer loading position where the light beam transmits through the jig wafer **220**. Thus, the wafer loading position of the feeding robot is accurately set. After completing the setting operation, the jig wafer **220** is removed so as to carry out a continuous feeding operation for wafers to be processed.

FIG. **10** illustrates an apparatus for controlling the supply of a coating solvent upon coating a photoresist solution over the surface of a wafer by the spin coater prior to the baking process. As shown in FIG. **10**, the coating solvent supply control apparatus includes a lamp **300** for irradiating an LED light beam onto the central portion of a wafer W loaded on the spin coater and rotated by the spin coater. A CCD camera **310** is arranged in the vicinity of the lamp **300** in such a fashion that it is focused onto an observation area A on the wafer W. A CCD controller **320** is coupled to the CCD camera **310**. The CCD controller **320** serves to control the turn-on and turn-off of the lamp **300** during a low-speed rotation of the spin coater **3**. The CCD controller **320** also recognizes an initial contrast of the wafer W and checks, based on the recognized initial contrast, a variation in contrast occurring in the observation area A when a coating solvent injected onto the surface of the wafer is diffused along the wafer surface. The CCD controller **320** detects such a variation in contrast in the form of an image. A main controller **340** is coupled to the CCD controller **320**. The main controller **340** receives an image signal from the CCD controller **320**, which signal is indicative of a variation in contrast detected by the CCD controller **320**. Based on the received image signal, the main controller **340** controls the operations of a variety of operating units including the lamp **300**, CCD camera **310**, a nozzle **330** adapted to inject the coating solvent, etc.

Accordingly, the coating solvent supply control apparatus having the above configuration detects the coated or injected state of the coating solvent, thereby controlling the supply of the coating solvent while controlling the rotating operation of the spin coater **3**. Therefore, it is possible to achieve a stable photoresist coating while using a reduced amount of solvent. Since there is no excessive consumption of solvent, it is also possible to reduce the costs. In accordance with the configuration of the coating solvent supply control apparatus, it is easy to vary the position of the observation area where the coated or injected state of the coating solvent is detected. It is also possible to reduce the time taken for the setting and change of detection conditions. As a result, various limitations, which result from the characteristics of the solvent used and the surface condition of the wafer, can be completely eliminated.

Referring to FIG. **11**, a stocker **400** is illustrated which is provided at the second interface **IF2** arranged between the spinner, in which a baking process is carried out, and the stepper **70**. Wafers W completely processed by the photoresist coating and developing processes are stocked in the stocker **400** of the second interface **IF2**. In order to store those wafers, the stocker **400** has a plurality of stock compartments **410** arranged in a multi-layered fashion. Each stock compartment **410** is open at both sides thereof so as to allow wafers to have access to the stock compartment **410** at both sides of the stock compartment **410**. A pair of wafer feeding arms, which are denoted by the reference numeral **140**, are arranged at both sides of the stocker **400**, respectively, in order to stock wafers in the stocker **400** at both sides of the stocker **400**.

Since the stocker **400**, which is arranged between the spinner and second interface **IF2**, has a configuration capable of achieving simultaneous stocking or removal of wafers at both sides of the stocker **400**, it is possible to more rapidly stock wafers continuously fed to the stocker **400** without any wafer pileup phenomenon. Accordingly, an improvement in productivity is achieved.

Thus, the present invention, which is adapted to configure the spinner itself and various units of the spinner to have multi-layered arrangements, is an epochal technique capable of achieving improvements in system installation, manufacturing processes, and system and process management, taking into consideration the fact that the entire installation volume and the number of processing units increase inevitably due to the use of new techniques coping with the enlargement of the standard (diameter) of wafers from the size of 6 or 8 inch to the size of 12 to 16 inch.

Although the numbers of bake units and spin units such as spin coaters and spin developers increase, it is possible to effectively increase the utility of the entire occupying space by virtue of the multi-layered arrangements of those installations according to the present invention. The movement range of each feeding robot for each processing unit can also be reduced. This results in a reduction in the operating load and time of the feeding robot.

As apparent from the above description, the present invention provides a semiconductor wafer processing system including wafer processing units arranged in a multi-layered fashion, thereby being capable of achieving a reduction in the occupying space of the entire installation. The semiconductor wafer processing system also has a configuration capable of achieving accurate wafer feeding and loading operations, and reducing the consumption of a chemical solvent coated over wafers. Accordingly, the present invention provides an economical and efficient semiconductor wafer processing system capable of achieving an improvement in productivity.

In accordance with the present invention, even when it is required to increase the number of processing units used or to introduce a new installation due to the use of new techniques, it is possible to minimize the occupying space of the entire system by virtue of the multi-layered arrangement of those processing units. In addition, the operating load and time of robots operatively associated with processing units can be reduced.

Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

What is claimed is:

1. A semiconductor wafer processing system comprising:

a first robot arranged downstream, in a feeding direction of wafers being processed, from an indexer carrying out wafer loading and unloading operations and adapted to feed a wafer loaded in the indexer to a desired one of processing units;

a first group of modules arranged in opposite sides of the first robot, the modules of the first module group being selected from first and second modules;

a second robot arranged downstream from the first robot in the wafer feeding direction via a first interface in such a fashion that it is aligned with the first robot in the wafer feeding direction;

a second group of modules arranged in opposite sides of the second robot, the modules of the second module group being selected from the first and second modules; and

a stepper arranged downstream from the second robot via a second interface in the wafer feeding direction and adapted to expose to light the entire portion of a wafer coated with a photoresist and fed thereto.

2. The semiconductor wafer processing system according to claim **1**, wherein:

each of the first modules comprises a plurality of bake units each having a plurality of bake boxes arranged in a multi-layered fashion, the bake units being arranged in such a fashion that they are adjacent to one another in the wafer feeding direction, and a spin unit fixedly mounted on the bake units, the spin unit comprising a spin coater or a spin developer; and

each of the second modules comprises a plurality of wafer edge exposure units arranged in a multi-layered fashion while being arranged in such a fashion that they are adjacent to one another in the wafer feeding direction, each of the wafer edge exposure units serving to expose to light an unnecessary portion of the photoresist disposed on the peripheral edge portion of each wafer, and a spin unit fixedly mounted on the wafer edge exposure units, the spin unit comprising a spin coater or a spin developer.

3. The semiconductor wafer processing system according to claim **2**, wherein each of the bake boxes comprises a pair of thermal plates arranged side by side with each other, each of the thermal plates being selected from a hot plate adapted to heat a wafer and a cool plate adapted to cool a wafer in such a fashion that the thermal plates of each bake box have the same type or different types, respectively.

4. The semiconductor wafer processing system according to claim **1**, wherein:

the modules of each of the module groups are also arranged in a multi-layered fashion to form at least two module layers and have the same module type or a combination of different module types;

each of the module groups constitutes a station, together with feeding means; and

a feeding interface or buffer stocker is arranged between adjacent stations respectively associated with the module groups.

5. The semiconductor wafer processing system according to claim 3, further comprising:

a plurality of support pins extending through vertical holes provided at each thermal plate of each of the bake units in such a fashion that they move vertically through the vertical holes while supporting a wafer thereon;

a cylinder for vertically moving the support pins between a loading position, in which the wafer supported by the support pins is loaded on the thermal plate, and an unloading position, in which the wafer is unloaded from the thermal plate;

a feeding robot arranged in the vicinity of the bake units, the feeding robot serving to carry out loading and unloading operations for wafers with respect to each of the bake units; and

a feeding arm arranged in a space defined between the thermal plates of each of the bake units and independently driven by separate drive means in such a fashion that it moves pivotally between the thermal plates, the feeding arm being provided at a free end thereof with a wafer holding member adapted to hold a wafer loaded in the bake unit.

6. The semiconductor wafer processing system according to claim 5, further comprising:

a position sensor arranged in the vicinity of the support pins associated with each of the thermal plates and adapted to sense a moved position of the support pins; and

a controller coupled to the position sensor and adapted to control the cylinder, based on an output signal from the position sensor, in such a fashion that the support pins supporting a wafer move at a high speed at an initial stage of a downward movement thereof for loading the wafer on the associated thermal plate and at a low speed at a stage of the downward movement thereof just before the wafer comes into contact with the thermal plate while moving at a high speed when they are separated from the wafer.

7. The semiconductor wafer processing system according to claim 5, further comprising:

a cover member arranged above each of the thermal plates in such a fashion that it moves vertically with respect to the thermal plate, thereby opening and closing the thermal plate; and

a cylinder adapted to move the cover member between a position, where the cover member opens the thermal plate, and a position, where the cover member closes the thermal plate, the cylinder operating independently of the cylinder adapted to drive the support pins.

8. The semiconductor wafer processing system according to claim 5, wherein the feeding robot comprises a pair of wafer feeding arms each adapted to feed a wafer to a desired position while holding the wafer, one of the wafer feeding arms having a plate shape and serving to support a peripheral portion of the wafer with the other wafer feeding arm having a bar shape and serving to support a portion of the wafer extending diametrically through the center of the wafer, so that a selected one of the wafer feeding arms operates to feed the wafer in accordance with the characteristics of a processing unit, in which the wafer is loaded.

9. The semiconductor wafer processing system according to claim 8, further comprising means for setting a wafer loading position of the feeding robot, the means comprising:

a reflex sensor arranged on an upper surface of each bake unit at a position corresponding to the center of a wafer accurately loaded on the upper surface of the bake unit in such a fashion that it radiates a light beam onto the center of the accurately loaded wafer; and

a jig wafer loaded in the bake unit by the feeding robot when it is desired to set a wafer loading position of the feeding robot, the jig wafer being provided at a central portion thereof with a through hole allowing a light beam to transmit therethrough;

whereby the wafer loading position of the feeding robot is accurately set to correspond to a desired wafer loading position, based on a signal, generated from the reflex sensor, indicative of whether a light beam emitted from the reflex sensor transmits through the through hole of the jig wafer loaded by the feeding robot or reflects from the jig wafer.

10. The semiconductor wafer processing system according to claim 1, further comprising:

a stocker provided at the second interface arranged between a spinner, in which a baking process is carried out, and the stepper, the stocker having a plurality of stock compartments arranged in a multi-layered fashion and adapted to stock wafers completely processed by photoresist coating and developing processes; and

a pair of wafer feeding arms arranged at opposite sides of the stocker, respectively, to stock wafers in the stock compartments of the stocker at the opposite sides of the stocker.

11. The semiconductor wafer processing system according to claim 2, wherein:

the modules of each of the module groups are also arranged in a multi-layered fashion to form at least two module layers and have the same module type or a combination of different module types;

each of the module groups constitutes a station, together with feeding means; and

a feeding interface or buffer stocker is arranged between adjacent stations respectively associated with the module groups.

12. The semiconductor wafer processing system according to claim 5, further comprising:

a stocker provided at the second interface arranged between a spinner, in which a baking process is carried out, and the stepper, the stoker having a plurality of stock compartments arranged in a multi-layered fashion and adapted to stock wafers completely processed by photoresist coating and developing processes; and a pair of wafers feeding arms arranged at opposite sides of the stocker, respectively, to stock wafers in the stock compartments of the stocker at the opposite sides of the stocker.

13. The semiconductor wafer processing system according to claim 6, further comprising:

a stocker provided at the second interface arranged between a spinner, in which a baking process is carried out, and the stepper, the stoker having a plurality of

stock compartments arranged in a multi-layered fashion and adapted to stock wafers completely processed by photoresist coating and developing processes; and a pair of wafers feeding arms arranged at opposite sides of the stocker, respectively, to stock wafers in the stock compartments of the stocker at the opposite sides of the stocker.

14. The semiconductor wafer processing system according to claim **7**, further comprising:

a stocker provided at the second interface arranged between a spinner, in which a baking process is carried out, and the stepper, the stoker having a plurality of stock compartments arranged in a multi-layered fashion and adapted to stock wafers completely processed by photoresist coating and developing processes; and a pair of wafers feeding arms arranged at opposite sides of the stocker, respectively, to stock wafers in the stock compartments of the stocker at the opposite sides of the stocker.

15. The semiconductor wafer processing system according to claim **8**, further comprising:

a stocker provided at the second interface arranged between a spinner, in which a baking process is carried out, and the stepper, the stoker having a plurality of stock compartments arranged in a multi-layered fashion and adapted to stock wafers completely processed by photoresist coating and developing processes; and a pair of wafers feeding arms arranged at opposite sides of the stocker, respectively, to stock wafers in the stock compartments of the stocker at the opposite sides of the stocker.

16. A semiconductor wafer processing system comprising means for controlling the amount of a coating solvent supplied when a photoresist solution is coated over a wafer, the means comprising:

a lamp for irradiating an LED light beam onto a central portion of a wafer loaded on a spin coater and rotated by the spin coater;

a CCD camera arranged in the vicinity of the lamp in such a fashion that it is focused onto an observation area defined on the wafer;

a CCD controller coupled to the CCD camera, the CCD controller controlling turn-on and turn-off states of the lamp during a low-speed rotation of the spin coater, recognizing an initial contrast of the wafer, checking, based on the recognized initial contrast, a variation in contrast occurring in the observation area when the coating solvent injected onto the wafer is diffused along the wafer, and detecting the variation in contrast in the form of an image; and

a main controller coupled to the CCD controller, the main controller receiving an image signal, generated from the CCD controller, indicative of the variation in contrast detected by the CCD controller, and controlling the operations of a variety of operating units including the lamp, the CCD camera and a nozzle adapted to inject the coating solvent.

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